DESIGN AND FABRICATION OF MICROMACHINED RADIO-FREQUENCY CAVITY RESONATORS

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By

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September 2006

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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September 2006

Resonators are used almost in every wireless communications applications and play an important role in the performance of these systems. At radio frequencies, for high performance applications, realization of high-Q resonators is required. Furthermore, in the near future, integration of RF resonators with rest of the system is intended. This thesis describes the design and fabrication of a type of radio-frequency MEMS cavity resonator operating in the frequency range of 2-3 GHz. The fabricated resonators are small in size so that they allow the integration of a whole system on a single-chip. The cavity is realized by selectively removing (etching) silicon substrate using standard MEMS techniques. The resonator is based on creating a low-loss inductor by enclosing the inductor in a metal-coated cavity and then resonating it with either a fixed or tunable high-Q capacitor. In this thesis, formulas for the inductance and the Q-factor of the cavity are derived and a number of resonators are fabricated and measured. The Q-factors of the measured cavities were found to be in the range going up to 25-30. The obtained results are promising and showed that on-chip resonators with

Q-factors higher than 30 can be realized based on this design and fabrication technique at this frequency range.

Keywords: RF-MEMS, Cavity Resonators, Cavity Inductors, MIM Capacitors, Quality Factor

ÖZET

MİKROİŞLENMİŞ RADYO-FREKANS KOVUK ÇINLAYICILARIN TASARIMI VE ÜRETİMİ

Cihan Hakan Arslan
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
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Eylül 2006

Çınlayıcılar hemen hemen bütün kablosuz haberleşme uygulamalarında kullanılırlar ve sistemlerin başarımında önemli rol oynar. Radyo frekanslarında çalışan yüksek başarım sistemleri için yüksek nitelik oranına sahip çınlayıcılar gerçekleştirmek gereklidir. Hatta, yakın bir gelecekte radyo frekans çınlayıcılarının, sistemlerin diğer parçalarıyla birlikte tümleşik hale getirilmesi düşünülmektedir. Bu tezde 2-3 GHz aralığında çalışan, radyo frekans MEMS ("Microelectromechanical Sytems") kovuk çınlayıcıların tasarımı ve üretimi anlatılmıştır. Üretilen çınlayıcılar, bütün sistemin tek bir kırmık üzerine tümdevre halinde gerçekleşmesine olanak verecek kadar küçük boyuttadır. Kovuk standart MEMS teknikleri kullanılarak silisyum pulunun aşındırılmasıyla elde edilmistir. Kovuk çınlayıcısı, metal kaplanmış kovuk tarafından çevrelenen düşük kayıplı indükleç ile sabit ya da değişken sığanın birbiriyle çınlatılması yoluyla meydana gelmiştir. Bu tezde kovuk için indükleç ve nitelik oranı değerleri hesaplanmıştır. Ölçülen kovuk çınlayıcısının nitelik oranı 25-30 arasında bulunmuştur. Bu tezde yapılan çalışmalar, diğer sistem elemanlarıyla tek kırmık üzerine inşa edilebilecek, nitelik oranları 30'dan fazla olan ve yüksek frekansta çalışan kovuk çınlayıcılar üretilebileceğini göstermektedir.

Anahtar Kelimeler: RF-MEMS, Kovuk Çınlayıcısı, Kovuk İndükleçi, Metal-yalıtıcı-metal sığası, Nitelik Oranı

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To My Ezgi and My Family ...

Chapter 1

INTRODUCTION

Radio-frequency wireless communication systems have been growing rapidly in order to satisfy the demand arising from military and commercial applications. This rapid growth brings many additional improvements together, such as smaller size, higher data transfer rate, better quality of service, *etc.* to these systems. However, most of these improvements require increase in operating frequencies of systems and their building blocks. Examples of such systems range from wireless LAN, bluetooth, satellite transponders and terresterial TV broadcast to military and civilian radio links. These wireless systems increasingly need both tunable and more stable frequency sources with less phase noise. It is estimated that the phase noise of a VCO is inversely proportional with the square of the quality factor (Q) of the resonator used in the VCO [2].

Using microelectromechanical systems (MEMS) techniques and silicon as a substrate, RF-MEMS resonators have been realized at frequencies above 2 GHz. MEMS technology offers many improvements on RF performance of silicon and makes possible to fabricate miniature size, integrated resonators on a substrate. The ultimate goal is to integrate the whole system on a single chip [2]. One of the approaches is to fabricate receiver architectures such that the external IF

filtering and external varactor-tuned LC resonators of the VCOs are replaced by resonators which are integrated with the rest of the system in a chip [3]. In recent years, a large effort has been dedicated to design and optimization of on-chip RF spiral inductors [4, 5, 6]. The associated capacitors, generally, exhibit higher quality factor than that of the inductors. Therefore, at 2 - 10 GHz, fabrication of high-Q on-chip inductors is of prime importance.

In this thesis, a high-Q inductor, which is intended to be used in VCO circuits, is developed using silicon. In on-chip inductors, the main loss mechanism is caused by the substrate due to the varying fields. The high-Q inductor can be realized by selectively removing the silicon substrate. Therefore, in this work, the inductor is enclosed within a cavity, which is fabricated inside the bulk silicon. The inductor is designed such that one of its terminals is grounded. The cavity is achieved by bonding two etched substrates face to face. MEMS techniques were employed, during etching of substrates. The associated capacitor was fabricated on top of the cavity and connected to the cavity inductor in parallel. The capacitor was an ordinary metal-insulator-metal capacitor, in which Si_3N_4 and BCB materials were tried as an insulator layer. Measurements were carried out using RF probes that were connected to Hewlett Packard 8753D Vector Network Analyzer.

The thesis starts with the introduction in which the motivation and the relevant background about the thesis are presented. In chapter 2, the definition of the terms and the theory of the work are explained. Chapter 3 starts with the design of the resonator structure. Then, physical dimensions and the fabrication steps of the device are discussed. Measurements of the fabricated devices are presented in chapter 4. The chapter also shows photographs taken during fabrication. And finally, in chapter 5 the conclusions and the future works are drawn.

Chapter 2

THEORY

2.1 Resonators: General View

Resonators are used in almost every communication system. For circuits that are operating at frequencies below 0.5 GHz, conventional lumped - element resonators and SAW devices are used along with other solutions to provide, both, low-cost and high performance. At microwave frequencies, transferring electromagnetic energy using these conventional lumped - elements is unattainable resulting in significant degradation in overall system performance. At these frequencies, fabrication of high performance (high-Q) resonators are essential and still under investigation. In the past years, a waveguide enclosed by conducting walls were studied as a cavity resonator in terms of resonance frequency and quality factor, Q. These resonators can exhibit very high-Q at microwave frequencies since air-filled cavity prevents radiation leaks and dielectric losses [7, 8, 9, 10]. However, this type of cavity resonators are not integrable with the rest of the system on a chip due to their relatively large physical sizes [11, 12]. On the other hand, resonators constructed by connecting a micromachined spiral inductor on Si substrate and a MIM (metal-insulator-metal) capacitor in parallel, are small

in size (in the micrometer range) and, therefore, easy to integrate on a chip; but such spiral inductors are usually very lossy due to the conductor and substrate losses so that high-Q resonator can not be obtained [13, 14, 15, 16, 17, 18, 19, 20]. In this thesis, design and fabrication of a micromachined RF cavity resonator on a silicon substrate is described. In the following sections, first, a definition of quality factor and resonance frequency of a resonator are presented. Then the basic transmission line theory is presented, in which it is shown that a short-circuited transmission line can be modeled by an equivalent circuit with lumped elements. In the last section cavity inductors that are fabricated in this work are discussed in terms of equivalent model, quality factor, resonance frequency and the size of the resonator.

2.2 Q-factor and Resonance Frequency

A simple resonator consists of a series or parallel combination of an inductor and a capacitor. Figure 2.1 shows a resonator circuit in which an inductor and a capacitor connected in parallel. One of the figure of merit of a resonator is its quality factor, Q_{res}, which is limited by the quality factor of inductor, Q_L and quality factor of the capacitor, Q_C. The parasitics in an inductor and a capacitor, due to the nature of materials they are created from, possess frequency dependent resistance, which results in ohmic losses. The fundamental definition of Q is [21]

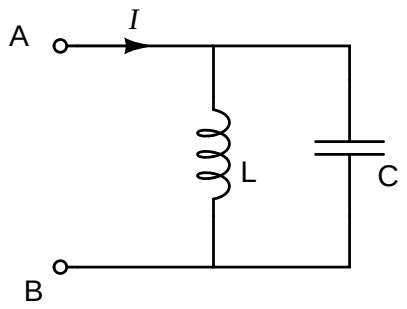


Figure 2.1: Parallel LC circuit.

$$Q = 2\pi \frac{\text{maximum stored energy}}{\text{energy loss in one oscillation cycle}}. \tag{2.1}$$

For an ideal inductor and capacitor, there will be no energy loss in the system and Q_L and Q_C are infinite. A real inductor can be represented by a series combination of an ideal inductor, L_s and a parasitic resistor R_s, as shown in figure 2.2(a). Then, the quality factor of the real inductor can be calculated from

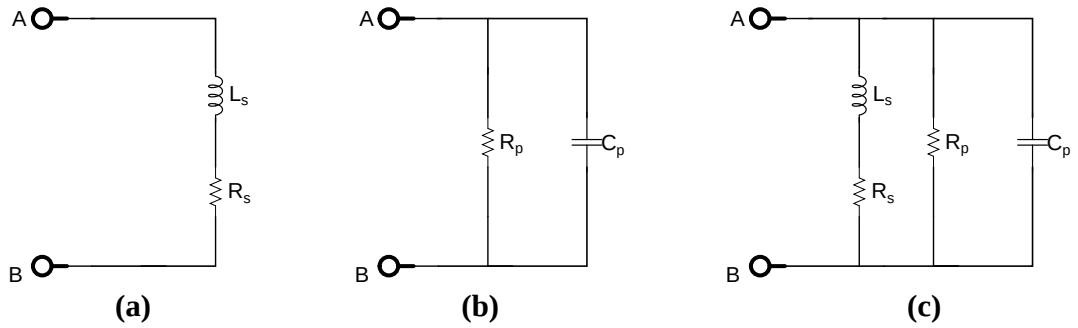


Figure 2.2: Inductors and capacitors, in practice, dissipate ohmic loss due to internal parasitic resistances

equation 2.1. In figure 2.2(a), the instantaneous stored energy in the inductor is,

$$E(t) = \frac{L_s\, i_L^2(t)}{2}. \tag{2.2}$$

For inductor current, $i_L(t) = I_p \cos \omega t$, (2.2) becomes,

$$E(t) = \frac{L_s\, I_p^2}{4}(1 + \cos 2\omega t) \tag{2.3}$$

and the peak stored energy as

$$E_{peak} = \frac{L_s\, I_p^2}{2}. \tag{2.4}$$

The energy dissipation in R_s in one cycle is

$$W_R = \int_0^T v_R(t) i(t)\, dt \tag{2.5}$$

$$= \int_0^T R_s I_p^2 \cos^2 wt\, dt \tag{2.6}$$

$$= \frac{I_p^2 R_s T}{2} \tag{2.7}$$

Thus,

$$Q_L = 2\pi \frac{I_p^2 L_s \omega}{2 I_p^2 R_s \pi} \tag{2.8}$$

$$= \frac{\omega L_s}{R_s}. \tag{2.9}$$

Similarly, a quality factor of a real capacitor in Figure 2.2(b) can be found as

$$E(t) = \frac{C_p\, v_C^2(t)}{2} \tag{2.10}$$

$$= \frac{C_p\, V_p^2}{4}(1 + \cos 2\omega t) \tag{2.11}$$

$$E_{peak} = \frac{C_p\, V_p^2}{2} \tag{2.12}$$

$$W_R = \int_0^T v_R(t) i(t)\, dt \tag{2.13}$$

$$= \int_0^T \frac{V_p^2}{R_p} \cos^2 wt\, dt \tag{2.14}$$

$$= \frac{V_p^2\, T}{2R_p} \tag{2.15}$$

$$Q_C = \omega C_p R_p. \tag{2.16}$$

where in (2.11), $v_C(t) = V_p \cos(\omega t)$.

When a real inductor and capacitor brought together, to form a resonant circuit, the overall quality factor, Q_{res} can be found in terms of Q_L and Q_C as

$$\frac{1}{Q_{res}} = \frac{1}{Q_L} + \frac{1}{Q_C}. \tag{2.17}$$

Consider Figure 2.2(c) in the case of $R_s = 0$, which means an ideal inductor is connected to a lossy capacitor. From equation 2.17, the quality factor of a

parallel RLC tank circuit is

$$Q_{res} = Q_C = \omega_0 R_p C_p. \tag{2.18}$$

Equation 2.17 implies that Q_{res} cannot be larger than neither Q_L nor Q_C. Both, Q of an inductor and Q of a capacitor must be high in order to achieve high-Q resonator. At microwave frequencies, it is not easy to construct high-Q devices since the parasitic effects increase with the frequency. Note that in equation 2.17 Q_L and Q_C are quality factors of L and C at resonance frequency, ω_0.

The resonance frequency is the frequency at which the imaginary part of the impedance of the resonator becomes zero. In Figure 2.2(c), when $R_s = 0$, the impedance of the parallel circuit seen from terminals A-B is given by [1]

$$Z_{res} = \frac{1}{\frac{1}{R_p} + \frac{1}{j\omega L_p} + j\omega C_p} \tag{2.19}$$

$$= \frac{1}{\frac{1}{R_p} + j[\omega C_p - \frac{1}{\omega L_p}]} \tag{2.20}$$

The imaginary term in the denominator of equation 2.20 equals to zero for

$$\omega = \omega_0 = \frac{1}{\sqrt{L_p C_p}} \tag{2.21}$$

which is the resonance frequency of the resonator.

2.3 Transmission Line Theory

Figure 2.3 shows a transmission line of length ℓ terminated with a load impedance, Z_L. The total input impedance, $Z_{in}(z = 0)$ is given by [22]

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh(\alpha + j\beta)\ell}{Z_0 + Z_L \tanh(\alpha + j\beta)\ell} \tag{2.22}$$

where Z_0, α and β are the characteristic impedance, attenuation constant and phase constant of the transmission line, respectively.

[1] it is convenient to define $L_p = L_s$ when $R_s = 0$

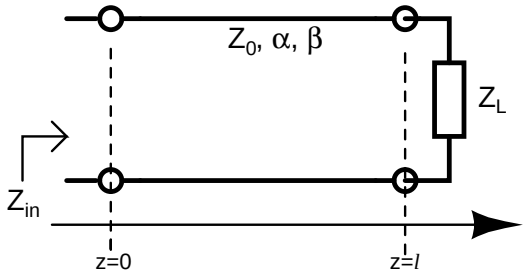


Figure 2.3: A transmission line terminated in a Z_L.

For a short-circuited transmission line ($Z_L = 0$), the equation 2.22 simplifies to

$$Z_{in} = Z_0 \tanh(\alpha + j\beta)\ell. \tag{2.23}$$

In the following sub-sections, equation 2.23 is examined separately in the cases of absence and presence of loss in the transmission line.

2.3.1 Lossless Transmission Line

To simplify the analysis consider the case when there is no loss in the transmission line ($\alpha = 0$). Now the input impedance (Z_{in}) becomes

$$\begin{aligned} Z_{in} &= Z_0 \tanh(j\beta\ell) && (2.24)\\ &= jZ_0 \tan(\beta\ell) && (2.25)\\ &= j\, Z_0\beta\ell. && (2.26) \end{aligned}$$

where last result was obtained by assuming $\beta\ell \ll 1$. We can observe that input impedance is purely imaginary in this case and for small $\beta\ell$, Z_{in} is purely inductive. The inductance of the equivalent circuit can be found from equation 2.26 and using the relation $Z_{in} = j\omega L$.

$$\begin{aligned} L &= \frac{Z_0\beta\ell}{\omega} && (2.27)\\ &= \frac{Z_0\ell}{\upsilon_p} && (2.28) \end{aligned}$$

where v_p is the phase velocity, which is constant for the lossless line and approximately constant for a low-loss line[22]. Equation 2.28 implies that for a relatively small ℓ with respect to the wavelength, λ, the transmission line exhibits an inductive behaviour and, moreover, the inductance value, L, stays constant with frequency as long as the condition $\frac{2\pi\ell}{\lambda} \ll 1$ holds. Figure 2.4 shows the equivalent circuit of a short- circuited lossless transmission line.

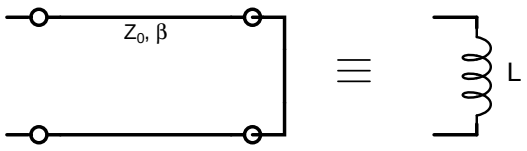


Figure 2.4: Equivalent circuit model of a lossless transmission line when $Z_L = 0$.

2.3.2 Lossy Transmission Line

In real life, transmission lines dissipate some energy due to finite conductivity and lossy dielectric between the inner and outer conductors. For a lossy transmission line, the attenuation constant, α, in equation $Z_{in} = Z_0 \tanh(\alpha + j\beta)\ell$, should be taken into account during analysis. If we apply an identity for the hyperbolic tangent for this equation, we get

$$Z_{in} = Z_0 \frac{\tanh(\alpha\ell) + j\tan(\beta\ell)}{1 + j\tan(\beta\ell)\tanh(\alpha\ell)}. \tag{2.29}$$

Again for the cases $\beta\ell \ll 1$ and $\alpha\ell \ll 1$ the input impedance simplifies to

$$Z_{in} = Z_0 \frac{\alpha\ell + j\beta\ell}{1 + j\,\beta\ell\,\alpha\ell}. \tag{2.30}$$

Further analysis leads to

$$Z_{in} = Z_0\,\ell\,\frac{(\alpha + j\beta)(1 - j\,\alpha\beta\ell^2)}{1 + (\alpha\beta\ell^2)^2} \tag{2.31}$$

$$= Z_0\,\alpha\,\ell\,\frac{1 + \beta^2\ell^2}{1 + (\alpha\beta\ell^2)^2} + j\,Z_0\,\beta\,\ell\,\frac{1 - \alpha^2\ell^2}{1 + (\alpha\beta\ell^2)^2}. \tag{2.32}$$

Note that if $\beta\ell \ll 1$ and $\alpha\ell \ll 1$ then $(\beta\ell)^2 \ll 1$ and $(\alpha\ell)^2 \ll 1$ also. Therefore the equation 2.32 can be re-written as

$$Z_{in} = Z_0\alpha\ell + j\, Z_0\beta\ell. \tag{2.33}$$

The equivalent circuit of a lossy transmission line is an inductor with a parasitic resistance in series. The inductance and the resistance values of the equivalent circuit are $L = \frac{Z_0\beta\ell}{\omega}$ and $R = Z_0\alpha\ell$, respectively. The loss in the line is represented by a series resistance, R, in this case. The inductance value of a lossy transmission line is the same as in equation 2.27, which is the inductance value of a lossless line. Figure 2.5 shows equivalent circuit of a short-circuited lossy transmission line. In the next section, cavities constructed from an air-filled

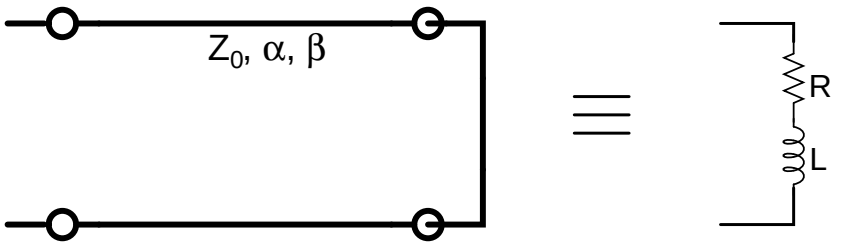


Figure 2.5: Equivalent circuit of a lossy transmission line when $Z_L = 0$.

waveguides are discussed. Since waveguides are also some sort of transmission lines, similar approaches can be applied in the analysis[23].

2.4 Cavity inductors

It was shown that a short-circuited transmission line of length ℓ, can be modeled as an inductor with a series resistance, for frequencies which satisfy the condition $\beta\ell \ll 1$. The same is true for a short-circuited waveguide also and for a cavity which is enclosed by conducting walls. In this thesis, cylindrical cavity constructed from copper plated walls and aluminium coated hexagonal cavity

formed by etching a silicon substrate using MEMS techniques are designed and fabricated. In this section theoretical results are presented for Q-factors and resonance frequencies of such resonators.

2.4.1 Cylindrical Cavity Inductor

Consider Figure 2.6 which shows an ordinary air-filled cylindrical cavity enclosed by conducting walls. There is a small circular slot at the left face ($z = 0$ plane). Energy is coupled to the cavity walls via a probe which passes through the slot and is connected to the right face of the cylinder (at $z = \ell$). Here, the objective is to find the impedance seen from terminals A and B so that the structure can be modeled by an equivalent circuit with lumped - elements. Note that, if the left and right faces are removed from the cylinder and if the probe is short-circuited by a small wire to the side wall at $z = \ell$, the cavity turns out to be a short-circuited coaxial transmission line, in which the probe forms the inner conductor and the side walls form the outer conductor of the transmission line.

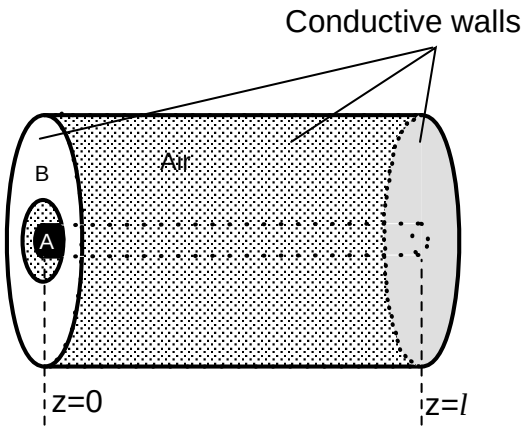


Figure 2.6: Air-filled cylindrical cavity

In section 2.3.2, it is found that the equivalent circuit of a lossy transmission line is an inductor and a resistor in series. The corresponding inductance and resistance values are also found in terms of transmission line characteristics. For

example, the series resistance, R, due to the loss in a line, is found as $R = Z_0\alpha\ell$. All these parameters depend on the transmission line characteristics; or by another way of saying, transmission line is characterized by these parameters. Here, Z_0 is the characteristic impedance of the line. For a coaxial transmission line, whose inner conductor radius is a and the outer conductor radius is b, the characteristic impedance, Z_0, is given by [23]

$$Z_0 = \frac{\eta \ln(b/a)}{2\pi} \tag{2.34}$$

where η is the intrinsic impedance of the medium and also given by in terms of permittivity and permeability of the medium as $\eta = \sqrt{\mu/\epsilon'}$. The attenuation constant, α, is another transmission line parameter and has two components: the attenuation due to the conductor loss, α_c, and the attenuation due to the lossy dielectric α_d. And for a coaxial transmission line α_c and α_d are given by [23]

$$\alpha_c = \frac{R_s}{2\eta \ln(b/a)}\Big(\frac{1}{a} + \frac{1}{b}\Big) \tag{2.35}$$

$$\alpha_d = \frac{1}{2}\beta \tan\delta \tag{2.36}$$

$$R_s = \sqrt{\frac{\pi f \mu_0}{\sigma}} \tag{2.37}$$

where R_s is the surface resistivity of an imperfect conductor. Here, it is worth to mention that in practice, the attenuation due to conductor loss is, generally, slightly bigger. This is because, in practice conductors do not have perfectly smooth surfaces. A rough surface causes a loss and therefore the attenuation increases. The following formula can be used to compensate the loss due to the surface roughness [24]

$$\alpha_c' = \alpha_c\left[1 + \frac{2}{\pi}\tan^{-1}\ 1.4\Big(\frac{\Delta}{\delta_s}\Big)^2\right] \tag{2.38}$$

where α_c' is the corrected attenuation constant for rough surfaces, Δ is the rms surface roughness, and δ_s is the skin depth of the conductor.

Note that for an air-filled line $\alpha_d = 0$ and $\alpha = \alpha_c$. From these results, a resistance, $R = Z_0\alpha\ell$, in the equivalent circuit model becomes

$$R = \frac{\eta \ln(b/a)}{2\pi}\sqrt{\frac{\pi f \mu_0}{\sigma}}\frac{1}{2\eta \ln(b/a)}\Big(\frac{1}{a}+\frac{1}{b}\Big)\ell \tag{2.39}$$

$$= \frac{1}{4}\sqrt{\frac{f\mu_0}{\pi\sigma}}\Big(\frac{1}{a}+\frac{1}{b}\Big)\ell. \tag{2.40}$$

Similarly, the inductance value, $L = \frac{Z_0\ell}{v_p}$, can be found as

$$L = \frac{\eta \ln(b/a)}{2\pi}\ell\sqrt{\mu\epsilon} \tag{2.41}$$

$$= \frac{\mu\ell \ln(b/a)}{2\pi}. \tag{2.42}$$

Now if we consider the air-filled cavity including with left and right faces as in the Figure 2.6, the impedance seen from port A and port B (which are shown in the figure) would be (not surprisingly) an inductor with an associated parasitic resistance. In this case, the equivalent resistance will be increased due to the power loss on the surfaces of left and right faces. It would be worth to say that in the previous discussion of lossy coaxial transmission line, energy loss through radiation was ignored. In a shielded cavity, the electromagnetic fields are completely confined inside the cavity and therefore, radiation losses are kept very low compared to coaxial transmission line.

Resistance of the left and right faces can be found from dissipated power on the surfaces. In Figure 2.7 current is generated at the center of the circular plate and flows in the radial direction. Here, it is assumed that the current flows in a very thin surface layer and therefore the corresponding current density, J_s approximately equals to J_{su}, surface current density. This is a good approximation as long as the conductivity of the faces and the operating frequency are very high; or skin depth is very low. Since there is power dissipation in the left and right faces, there should be non-zero radial electric field, $\mathbf{a_r E_r}$, at the surfaces in the same direction of J_{su}. Then the associated average Poynting vector would

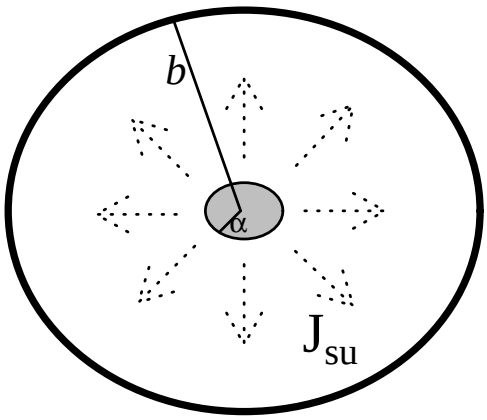


Figure 2.7: Power dissipation occurs on the surface of a imperfect circular conductor.

be

$$p_\sigma = \frac{1}{2}\,\Re\{|J_{su}|^2 Z_s\} \tag{2.43}$$

where Z_s is the intrinsic impedance of the surface and equals to [22]

$$Z_s = (1+j)\sqrt{\frac{\pi f \mu}{\sigma}} \tag{2.44}$$

for a good conductor. If we put equation 2.44 into equation 2.43, we get

$$p_\sigma = \frac{1}{2}\,|J_{su}|^2 \sqrt{\frac{\pi f \mu}{\sigma}}. \tag{2.45}$$

Surface current I is

$$I = \int_{\phi=0}^{2\pi} J_{su} r\, d\phi \tag{2.46}$$

$$= J_{su} 2\pi r \tag{2.47}$$

And the power dissipated on one of the faces is

$$P = \int_S p_\sigma\, ds \tag{2.48}$$

$$= \frac{1}{2}\sqrt{\frac{\pi f \mu}{\sigma}} \int_{\phi=0}^{2\pi}\int_{r=a}^{b} \frac{I^2}{(2\pi r)^2} r\, dr d\phi \tag{2.49}$$

$$= I^2 \frac{1}{4}\sqrt{\frac{f\mu}{\pi\sigma}}\ln(b/a). \tag{2.50}$$

Hence, the effective series resistance for one face is found as

$$R_{face} = \frac{1}{4}\sqrt{\frac{\mu f}{\pi\sigma}}\ln(b/a). \tag{2.51}$$

Similarly, from the complex power dissipated on the surface and using equation 2.44, the effective inductance can be found as

$$\omega L_{face} = \frac{1}{4}\sqrt{\frac{\pi f\mu}{\sigma}}\ln(b/a) \tag{2.52}$$

$$L_{face} = \frac{1}{8\pi}\sqrt{\frac{\mu}{\pi f\sigma}}\ln(b/a). \tag{2.53}$$

Note that this inductance can be negligible compared with the inductance value given in equation 2.42, when the conductivity of the surface and the operating frequency are high enough. Figure 2.8 shows the equivalent circuit of the cavity given in Figure 2.6. For total inductance, $L_T \approx L$, and total resistance, $R_T = R + 2R_{face}$ the quality factor, Q of the inductor will be

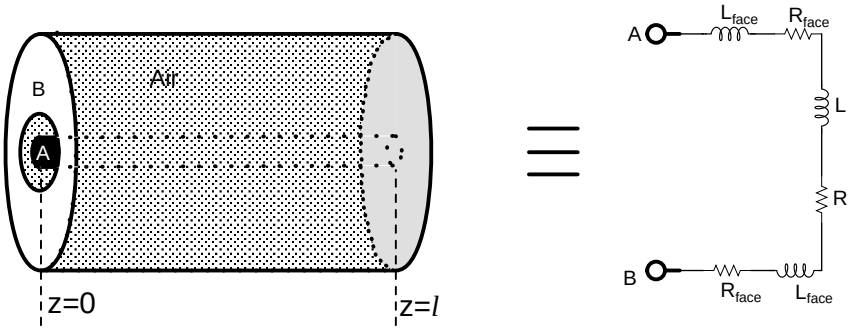


Figure 2.8: Equivalent circuit with lumped - elements.

$$Q = \frac{\omega L_T}{R_T} \tag{2.54}$$

$$= \frac{2\pi f \frac{\mu_0 \ell}{2\pi}\ln\frac{b}{a}}{\frac{1}{4}\sqrt{\frac{f\mu_0}{\pi\sigma}}\left(2\ln\frac{b}{a} + \frac{\ell}{a} + \frac{\ell}{b}\right)} \tag{2.55}$$

$$= 4\,\ell\sqrt{\mu_0 f \pi \sigma}\frac{\ln\frac{b}{a}}{2\ln\frac{b}{a}+\frac{\ell}{a}+\frac{\ell}{b}} \tag{2.56}$$

$$= \frac{4\,\ell}{\delta(f)}\,\frac{\ln\frac{b}{a}}{2\ln\frac{b}{a}+\frac{\ell}{a}+\frac{\ell}{b}} \tag{2.57}$$

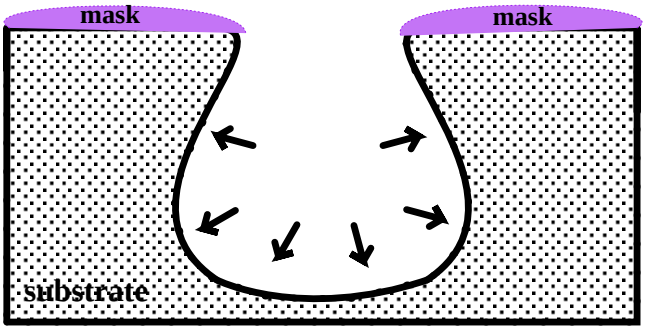
2.4.2 Silicon Cavity MEMS Inductor

In the previous section, a shielded cylindrical cavity is discussed. The structure is modeled by lumped circuit elements and parameters in the circuit model are found. In this thesis, another similar type of cavity was fabricated by micromachining silicon substrate. Silicon was used because it is easy to utilize MEMS techniques on it. By selectively removing (etching) substrate of the silicon, a cavity inside the substrate can be constructed. However, such a cylindrical cavity structure as in Figure 2.6 is very hard to achieve due to the nature of the crystallographic structure of Si. Therefore, not a cylindrical but hexagonal cavity was fabricated which is easier to realize. Here, the important thing is not the shape of the cavity but cavity itself. A cavity enclosed inductor has low-loss at high frequencies. On the other hand, in a printed inductor (when there is no cavity), losses due to the silicon substrate significantly reduce the performance of the device as the frequency increases. Thus, an inductor enclosed in an air-filled cavity is constructed to obtain a low-loss inductor.

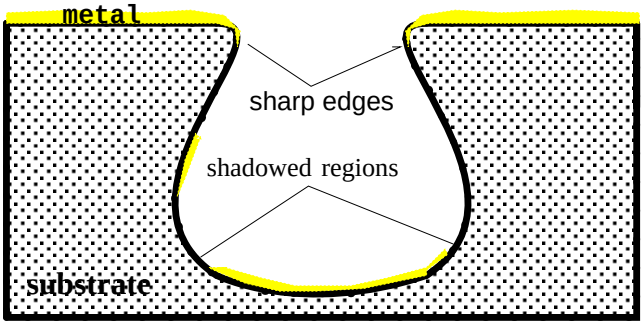
There are various silicon substrate etchants in the literature. Most common of them are HNA (hydrofluoric acid, nitric acid and acetic acid), EDP (ethylenediamine and pyrocatechol), TMAH (tetramethyl ammonium hydroxide), DRIE (deep reactive ion etch) and KOH (potassium hydroxide). Etching of a substrate in a liquid etchant such as HNA, EDP, TMAH and KOH is referred to as wet etching. On the other hand, DRIE is an example of dry etching where the etchants (reactants) are in plasma state. Etching processes are also catagorized in terms of being isotropic or anisotropic. Depending on the type of the

etchant and crystallographic structure of substrate the etching process can be either isotropic or anisotropic. In anisotropic etching, etch rates of different crystallographic planes differs, while in isotropic etching etch rates of different planes are equal. HNA etch of silicon is an example of isotropic etching where etchants attack to the silicon surface at the same rates in all directions. KOH etching of silicon is an example of anisotropic etching where etch rate in the $\langle 110 \rangle$ direction is about more than 500 times of the etch rate in the $\langle 111 \rangle$ direction which provides achieving of different shape of structures[25].

Since silicon is a poor conducting material, cavity walls must be shielded by a good conductor such as gold, copper, alminium, *etc.* The critical issue here is that after metal is plated to the walls of the cavity, the continuous electrical conductivity between the walls must be established, which is not so easy in some cases. The situation can be explained better from Figure 2.9. In the figure, substrate is selectively etched by using isotropic etchant and appropriate masking. However, during isotropic etching, as it is shown in the figure, some regions, which are under the etch mask, are also etched horizontally. This situation is often undesirable. In the isotropic etching, as reactants etch through the substrate, they attack in all directions at the same etch rate which makes isotropic etching impractical for some applications (as in our case). After etching of substrate is completed, a cavity is formed. However, as mentioned earlier, conductivity of a silicon substrate is very low and therefore the side walls must be deposited by a good conductor. During deposition of a metal (usually done by evaporation), undercut regions are shadowed by the masking area and metal could not be deposited onto those regions. Sputtering might help to solve this shadowing problem but it is still difficult to achieve a continuous conductivity at places where sharp edges found. On the other hand, anisotropic etching of silicon can also be utilized to construct a cavity inside the substrate. KOH (potassium hydroxide) and water mixture is well-known, frequently used wet etching solution. KOH etching of (100) silicon makes an angle of 54.7° between the plane



(a)



(b)

Figure 2.9: Isotropic etching and metal deposition (side view). (a) Same etch rate in all directions. (b) Unsuccessful metal deposition due to the sharp edges and undercut.

of the wafer and the {111} plane[26], as shown in Figure 2.10(a). Note that after metal deposition, in this case, electrical conductivity can be easily obtained between the cavity walls. However, now, from Figure 2.10(b) and Figure 2.11 it can be seen that the opening at the top surface of the silicon substrate becomes wider which can cause radiation loss.

Another issue is the depth of the cavity, ℓ, which is limited by the substrate thickness. In equations 2.42 and 2.57, the values of inductance, L, and the quality factor, Q, are proportional with the depth of the cavity. Thus, the deeper cavity means higher inductance and higher Q-factor. One of the possible approaches

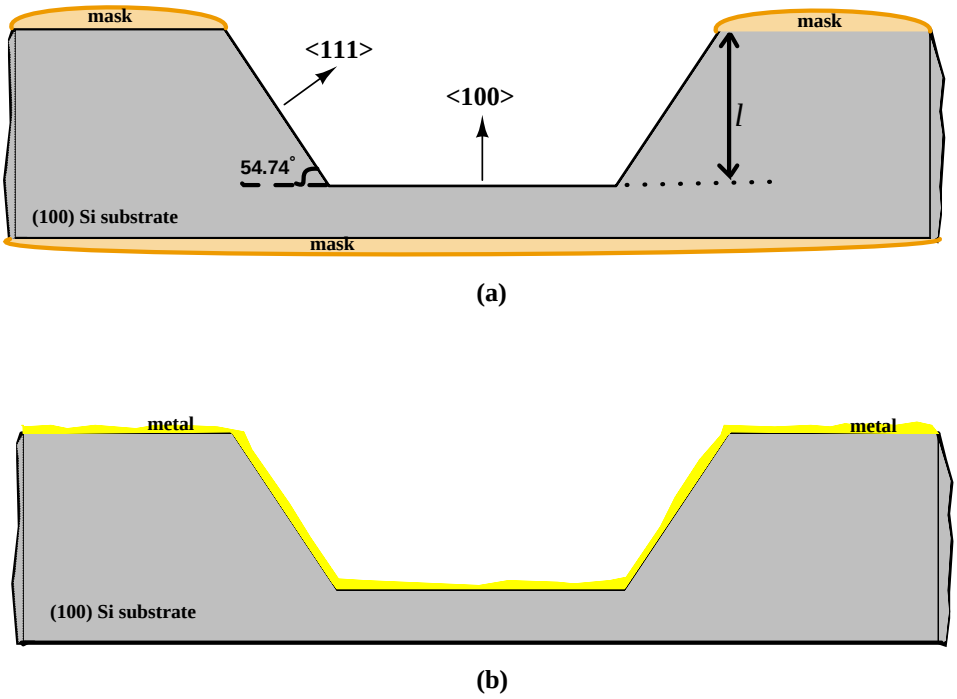


Figure 2.10: Anisotropic KOH etching of (100) Silicon and metal deposition (Side view). (a) Etch rate in ⟨100⟩ significantly larger than etch rate in ⟨111⟩ direction. (b) Successful metal deposition.

to increase the depth of the cavity is shown in the next figure. Here, KOH etched and gold (or any other metal) deposited Si substrate is turned upside down and placed on the top surface of another substrate. In this structure, the depth of the cavity increases twice while the opening becomes much narrower. By using this method, from bulk of the silicon, not cylindrical but hexagonal cavity with metallic walls can be fabricated. As in the cylindrical inductor, an opening can be made at the top of the substrate so that a probe is inserted into the cavity (Figure 2.12(b)). The final structure offers a high-Q MEMS inductor at microwave frequencies. In this thesis, the structures in Figures 2.8 and 2.12 are fabricated. The dimensions of the cavities are $a = 0.5$ mm, $b = 10$ mm, $\ell = 11$ mm and $a = 12.5$ μm, $b = 3000$ μm, $\ell = 900$ μm, respectively. The resonator circuit is achieved by connecting external chip capacitor in parallel to the terminals A and B of the cylindrical cavity.For the silicon cavity, a MIM

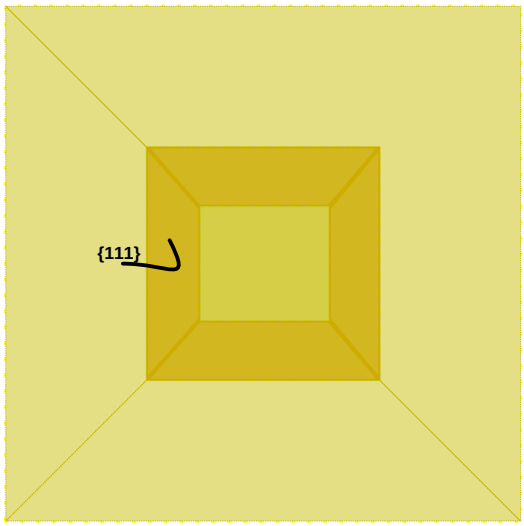
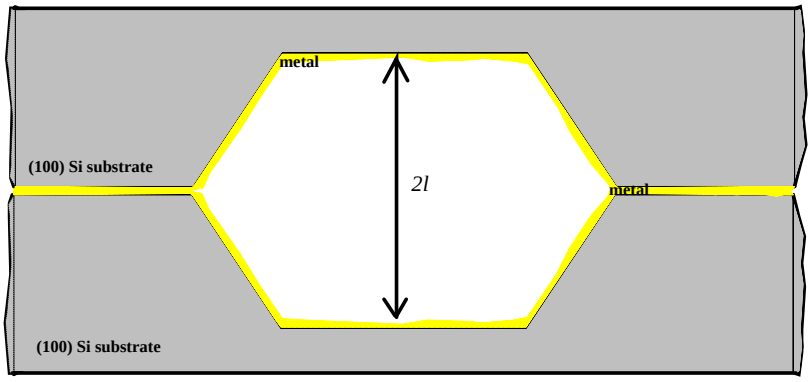
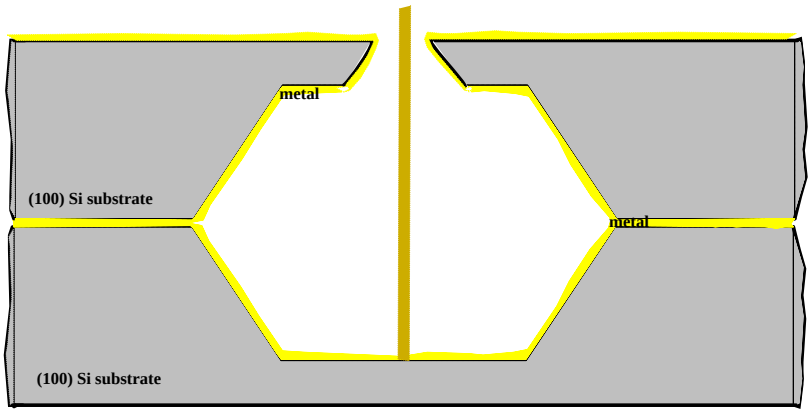


Figure 2.11: Anisotropic KOH etching of (100) Silicon. Metal is deposited to side walls of the cavity (Top view).

capacitor is fabricated on the top surface of the silicon substrate, next to the opening where probe is inserted. Note that the dimensions of the cylindrical cavity are very large compared to silicon cavity so that it cannot be integrated in a single chip. It is worth to mention that the purpose of the cylindrical cavity fabrication is to verify the equations that are found in 2.57 and 2.42. In the next chapter, the results of the cylindrical cavity is presented.



(a)



(b)

Figure 2.12: Two silicon substrate is combined face to face (Side view). (a) The cavity is formed. (b) An opening can be made at the top surface of the cavity to couple the energy.

Chapter 3

CONSTRUCTION AND MEASUREMENT RESULTS OF A LARGE SCALE CYLINDRICAL CAVITY RESONATOR

An air-filled cylindrical cavity was fabricated from 0.1 mm thick copper plate in order to verify the inductance and Q-factor equations given in chapter 2. The energy is coupled into the cavity via a SMA coaxial connector placed at the center of one of the side face of the short-circuited cavity. The probe of the SMA, penetrating into the cavity, was connected to the other side face of the cylinder. An external chip capacitor, is soldered between the probe and the ground of the SMA connector. The photographs taken during measurements can be seen from Figures 3.1, 3.2 and 3.3.

Figure 3.1: Photograph of cylindrical cavity.

The dimensions of the cylinder was as follows: $b = 10$ mm, $a = 0.5$ mm and $\ell = 11$ mm. From equations 2.57 and 2.42, the inductance value, L, and the corresponding quality factor, Q_L can be calculated as

$$\begin{aligned} L &= \frac{\mu_0 \ell}{2\pi} \ln(b/a) \\ L &= 6.59 \text{ nH} \\ Q(f = 1GHz) &= 2200 \end{aligned}$$

The capacitance value of the chip capacitor was 5.6 pF. The next four figures show the results of the measurements of cylindrical cavity resonator. Measurements were done by using HP 8753D Vector Network Analyzer.

The resonance frequency, f_{res}, was measured as 830 MHz. Then, the inductance value can be found as

$$L = \frac{1}{\omega_0^2 C} \tag{3.1}$$

$$L = 6.56 \text{ nH}. \tag{3.2}$$

Figure 3.2: Photograph of cylindrical cavity.

Note that, this value is very close to the computed inductance value using equation 2.42. On the other hand, the quality factor was measured as,

$$Q_L = \frac{f_{res}}{\Delta f_{3dB}} \tag{3.3}$$

$$Q_L = \frac{830}{6.5} \tag{3.4}$$

$$Q_L = 128 \tag{3.5}$$

which is far from the calculated value. Although every effort was undertaken to make the impedance measurement as precise as possible, the measurement accuracy was limited by the accuracy of the calibration sets. Even under these circumstances, the measured Q is very high and is obviously limited by the Q of the capacitor. The calculated value of the Q (2200) is very difficult to measure by using network analyzer at these frequencies and it is certainly beyond the scope of this thesis. The main obiective behind this exercise of building a large scale model was two-fold; to verify the inductance and quality factor formulas to some extend and to develop and try the Q measurement methodology. The

Figure 3.3: Photograph of cylindrical cavity.

result was encouraging, so we progressed to develop, fabricate and measure the actual on-chip resonator.

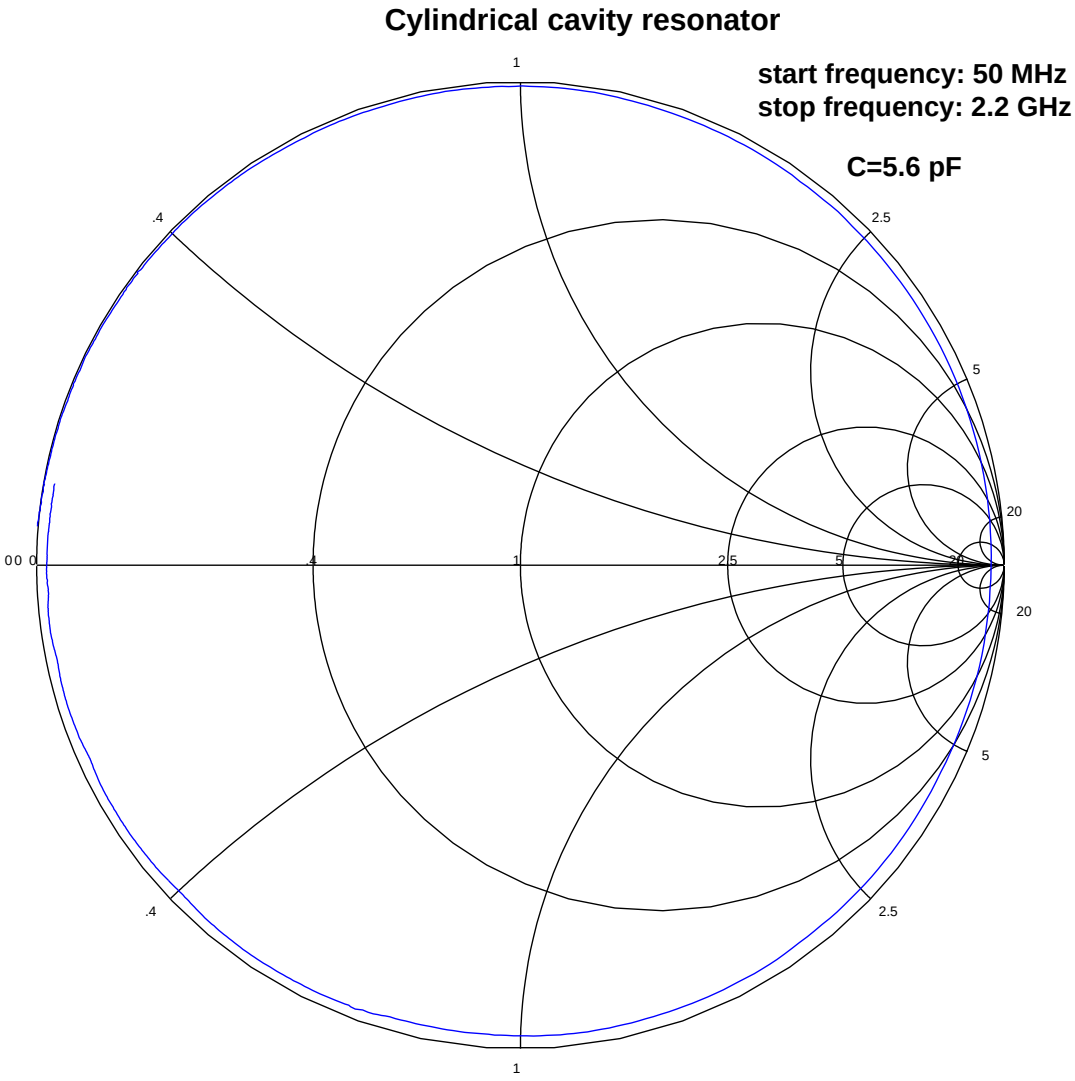


Figure 3.4: Smith chart plot of the cylindrical cavity resonator.

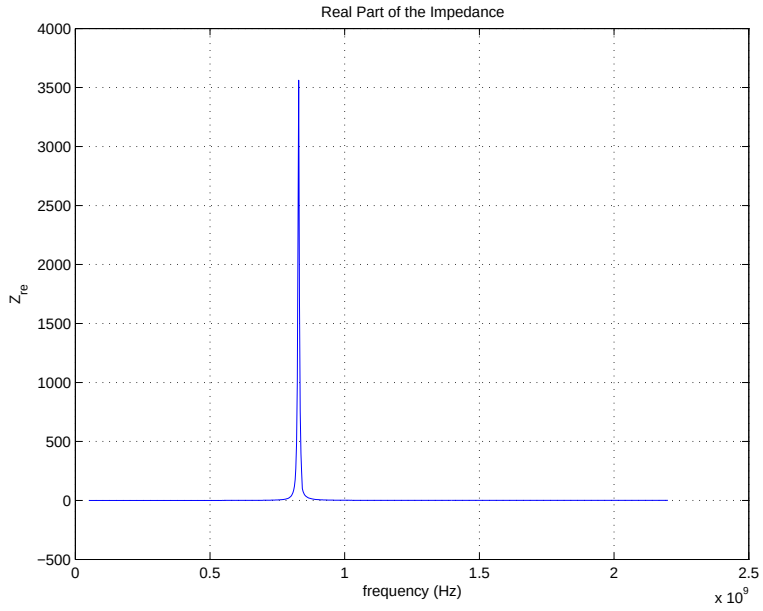


Figure 3.5: Real part of the impedance.

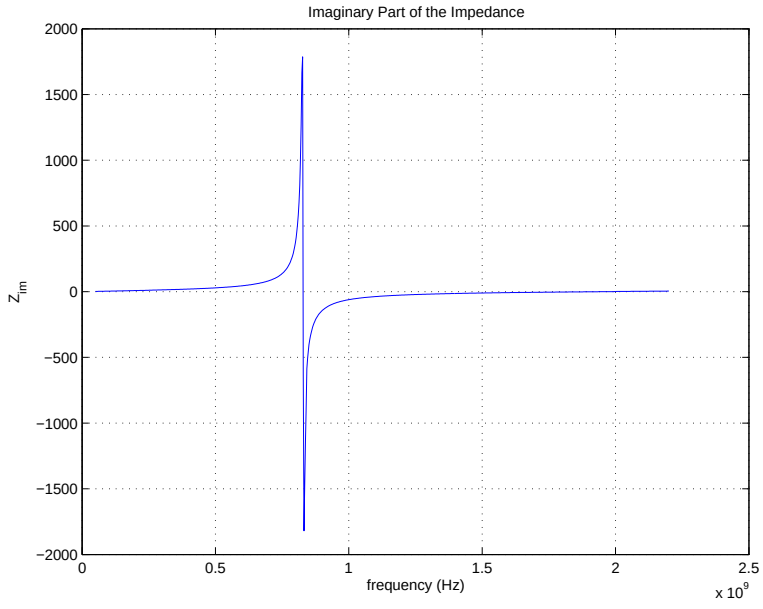


Figure 3.6: Imaginary part of the impedance.

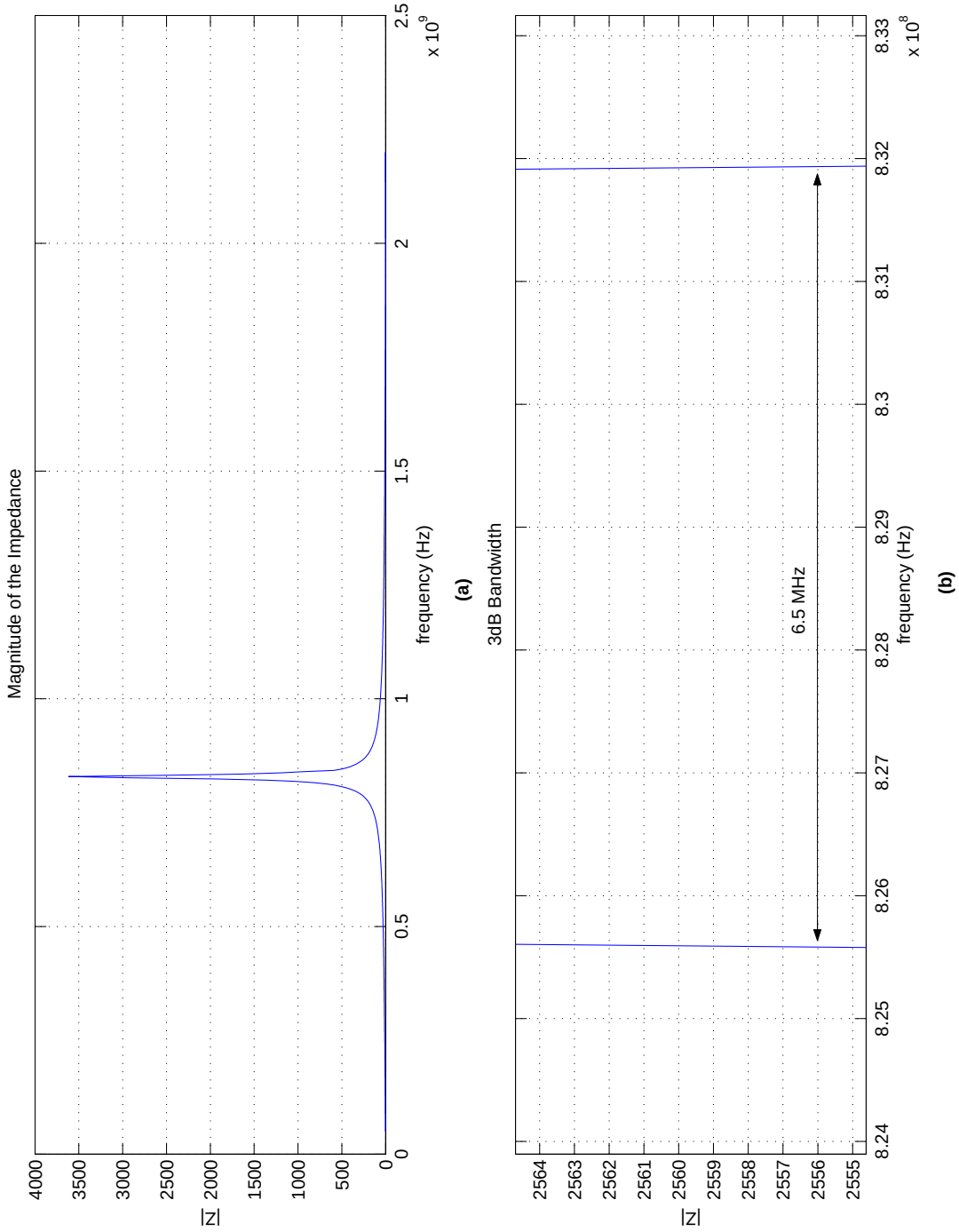


Figure 3.7: (a) Magnitude of the impedance. (b) 3dB bandwidth.

Chapter 4

DESIGN AND FABRICATION OF SILICON CAVITY RESONATOR

4.1 Device Design

At the beginnning of the project, different cavity structures were considered. Several of them are shown in Figure 4.1. Note that, in these structures it is possible to achieve completely enclosed cavities by bonding two etched substrates together. In the litreature, bonding of two wafers was realized by [27, 28, 29, 11, 14]. However, note also that cavity depths are limited by a thickness of a single wafer. The reason of this limitation is the following: just under the opening, a small part of the top surface is not removed by using an appropriate mask which causes a pyramid shape structure at the center of the substrate in KOH etching of (100) Silicon. Pyramidal structure is used as a probe to couple the energy into the cavity. Since the height of this structure should reach from bottom to top surface (which is the substrate thickness), the cavity depth cannot

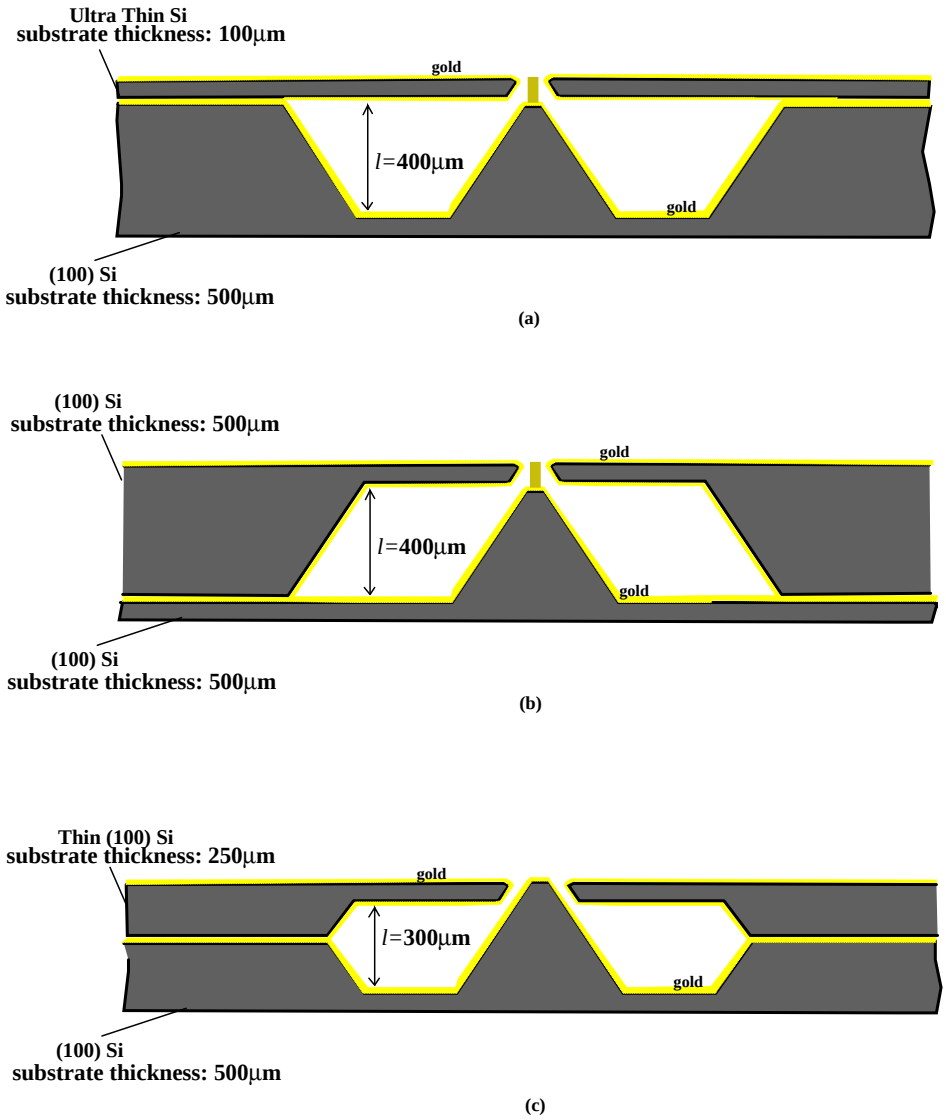


Figure 4.1: Silicon cavities achieved by bonding of two substrates.

exceed that limit. The base area of this structure becomes larger and the cavity becomes smaller as the substrate is etched further. This reduces the associated inductance value of the cavity. In fact, it is very hard to realize such a small pyramidal structure at the center of the cavity while etching down the substrate about 400 μm. This is because of undercutting of convex corners during KOH etching of Si. Corner compensation techniques are also not very practical in this case since the dimensions of the compensating structures exceed the dimensions of the cavity resulting in unsuitable masking of the substrate. Using a thick

wafer (such as a substrate thickness of 1000 μm) is not convenient due to the same problems. Therefore, these structures were omitted at the design stage and were not fabricated.

Consider the structure in Figure 4.2 where one end of the gold wire is con-

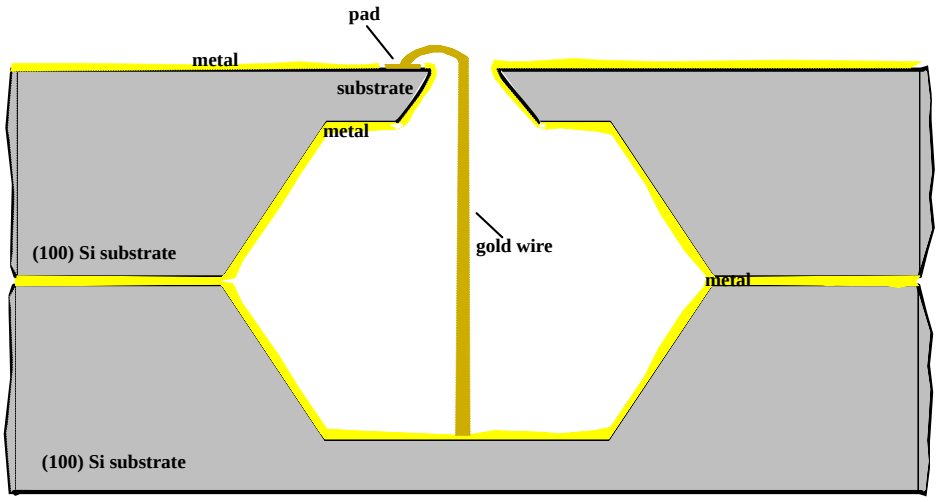


Figure 4.2: Initial design.

nected to the pad on top of the substrate while the other end is connected to the base of the substrate. Since lightly-doped silicon is poor conductor, at DC there is no electrical connection between the pad and the metal-coated walls through substrate. Obviously, there is a connection through the wire. This structure, compared to the ones in Figure 4.1 offers many advantages. As stated before, the cavity depth increases by two which significantly enhances the quality factor and the inductance value of the inductor. Energy is coupled via a gold wire, hence, there is no pyramid shape structure and consequently no convex corners compensation is needed. A low-cost, lightly-doped, typical silicon wafer having a thickness of 500 μm can be used for both top and bottom substrates. Therefore, we considered these advantages and decided to fabricate this structure. But, as shown in Figure 4.2, there is no capacitor in the structure. This is because in the design stage, our first intention was to fabricate high-Q inductor that can be

used at microwave frequencies rather than a resonator. A resonant circuit would be easily realized by connecting a high-Q chip capacitor or a varactor between the pad and the metal walls at the top surface.

During the fabrication of the above structure, we encountered some difficulties, however, and therefore, the structure was changed several times. The main problem was the substrate loss of silicon. When a signal was applied between the pad and the metal walls on the top surface, there was a significant loss due to the lossy substrate under the pad. Fields penatrating from the pad to the walls get experienced a substrate loss, which results in significant degradation in the quality factor of the inductor. This is shown in Figure 4.3. Note that metal-coated walls completely shield electromagnetic waves inside the cavity from the lossy substrate and thus, there was no such loss. Several approaches were used to pre-

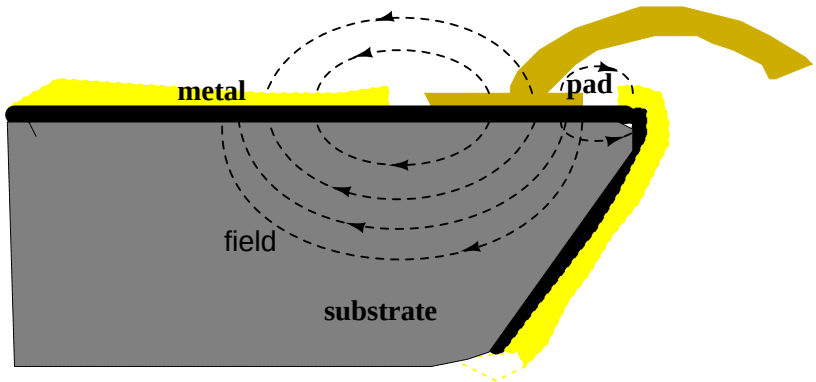


Figure 4.3: Substrate loss

vent the loss. One of them was coating a low-loss dielectric just under the pad. BCB (benzocyclobutane) was used for this purpose. BCB has been developed for high frequency MEMS applications by The Dow Chemical Company [30]. It is easy to coat and exhibit very small loss-tangent compared to silicon substrate.

As a result of this improvement, the loss becomes less but was still an unacceptable level. In chapter 5, the smith chart plots are given for each device tested. Then, PECVD silicon nitride was deposited as an alternative low-loss dilelectric instead of BCB, but almost similar results were obtained. A better approach was needed in the design to reduce the substrate loss. We decided to shield the entire top surface as we did at the cavity walls. At this point the structure turned out to be a resonator. Because a MIM (metal-insulator-metal) capacitor should be placed, in this case, to provide an isolation between the signal pad and the metallic walls on the top surface. And the parallel combination of the MIM capacitor and the inductor acts as a resonant circuit. The final structure is given in Figure 4.4. By this way, both reduction in loss and the realization of an on-chip resonator are established at the same time.

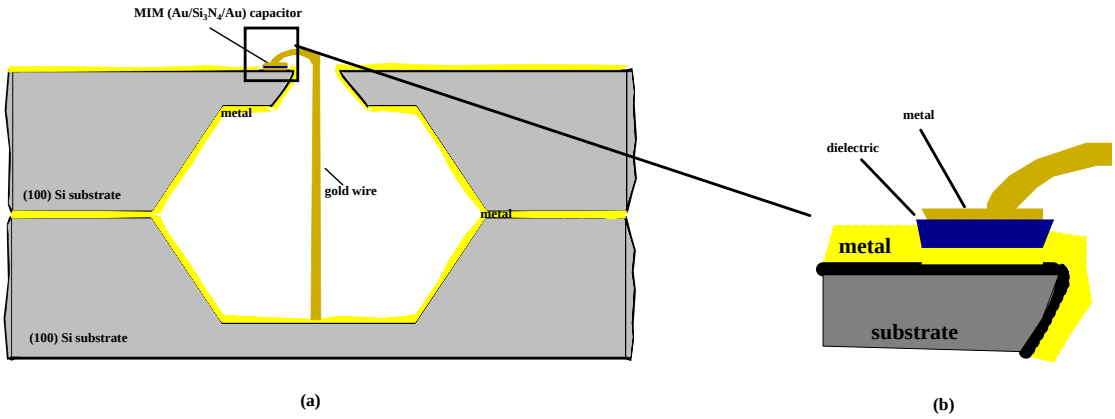


Figure 4.4: (a) RF MEMS Cavity Resonator. (b) MIM capacitor at the top of the cavity

There were also other problems which have effects on the performance of the device. For example, bonding of the gold wire shown in the structure at the bottom substrate requires vertical deep access wedge bonder or a ball bonder equipment. Therefore, the width of top opening must be sufficiently large for the bonding tool to access the deep cavity. Also, bonding onto the pad area was very problematic since the required force for making successful bonding was

strong enough to smash the MIM capacitor under the pad. Therefore, bonding to the top surface was done by using a silver epoxy which, certainly, causes a loss. Silver epoxy was also used in bonding of the two substrates although a better way of bonding two wafers is a thermocompression bonding as in [14]. Due to such limitations in the fabrication processes, the resonator was designed accordingly. As the future work, if these problems are solved, the quality factor of the resonator will be considerably enhanced.

This structure was fabricated in the Advanced Research Laboratories - Class 100 Clean Room. And the measurements were done by using HP 8753D Vector Network Analyzer in our department. Results showed that an on-chip high-Q resonator at microwave frequencies can be fabricated by using this geometry. Moreover, it is possible to make a tunable resonator if a MIM capacitor is replaced by a varactor. Also, Q-factor can be improved further by changing a few steps during fabrication.

4.2 Physical Dimensions of the Device

In this section, dimensions of the cavity, the gold wire and the capacitor is given. Theoretical values of the capacitance value, C, the inductance value, L, and the corresponding quality factor, Q_L and the resonance frequency, ω_0, of the resonator are also calculated using the equations given in chapter 2.

In Figure 4.4(a), the structure of the cavity resonator is given. In the figure, the width of the openning at the top surface seems very narrow compared to the depth of the silicon. However, as described in section 4.1, this opening should be large enough so that the bonding tool can be inserted from the opening and reach to the base of the cavity. Therefore, the width of this opening is limited by the tool that is used. There are special tools in the market for deep access bonding processes. For example Deweyl Tool Company provides vertical access

tool whose bottom width is only 230 μm which means an opening of 300-350 μm is fairly enough to insert the tool and make contact to the base[31]. However, in our case, Kulicke & Soffa ball bonder was available and used. In this manner, the opening had to be kept relatively larger. Figure 4.5 shows the dimensions of the structure. In the figure, the substrate thickness is given as 500 μm. The

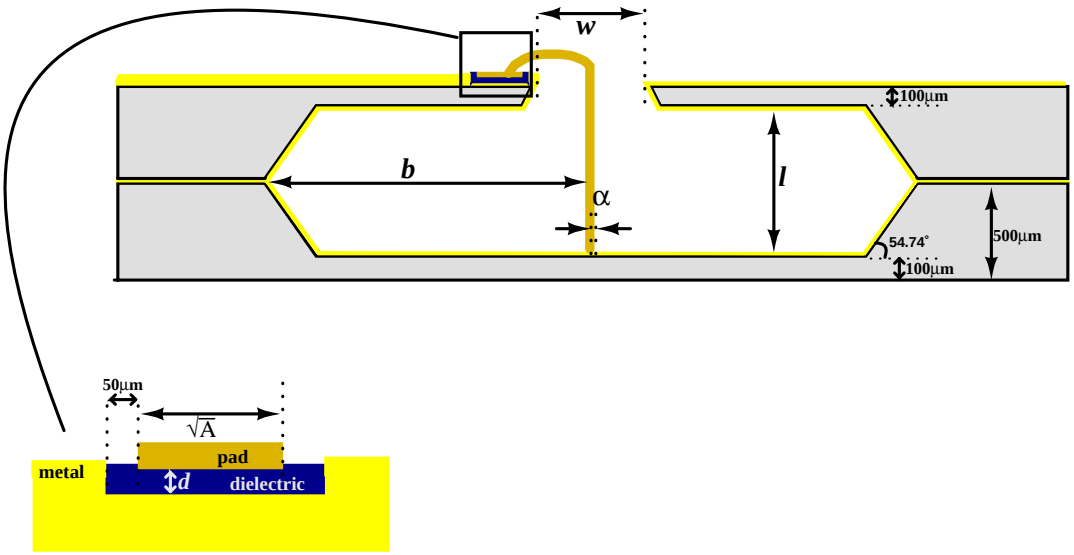


Figure 4.5: Physical dimensions of the cavity resonator (Side view).

bottom substrate is etched until a thickness of 100 μm left. Note that, the top substrate is completely etched away to make an opening at the surface. The width of the opening is denoted by w. In the fabrication, w was chosen to be about 650 μm. The depth and the radius of the cavity are denoted by ℓ and b, respectively. The radius of the wire, also, has an important effect on the values of inductance and Q-factor and denoted by a. From equation 2.57, it can be seen that a high-Q inductor can be realized by choosing the radius of the wire large which reduces the conductor loss. However, the bonding equipment that was used in this work is compatible with the wire of diameter 25 μm. Therefore, in our case, $a = \frac{25\ \mu\text{m}}{2}$ =12.5 μm. As shown in the figure, depth of the cavity, ℓ, is 900 μm. Finally, the radius of the cavity, b, can be chosen without any restriction. A single and trivial restriction on b might be size of the device. As b

increases, sizes of the device and chip also increase. In this thesis, b was chosen as 1500 μm. If these values of a, b, ℓ are put into equations 2.42 and 2.57, the approximate inductance and Q-factor values of the cavity can be calculated as,

$$L = 0.9 \text{ nH} \tag{4.1}$$

$$Q_L = 171 \tag{4.2}$$

at 4.5 GHz and for aluminium coated walls. Note that equations 2.42 and 2.57 are found for cylindrical cavity, not for the structure given in Figure 4.5. Another point is that, in this geometry the length of the gold wire is not equal to the depth of the cavity, which is the case in Figure 2.6. The length of the wire has, certainly, an effect on the inductance value L. Therefore, the theoretical calculations given in this section deviate from the experimental results.

The dimensions of the paralel-plate capacitor is also shown in Figure 4.5. Plates are in the shape of a square. The one edge of the square is given as $\sqrt{A}$, where A is the pad area. The capacitance value, C, is directly related with the size of A and the thickness of the dielectric material, d. As stated before, the pad area should be large enough to make a successful bonding of the wire. To serve this, the edge of the pad area was set to minimum 175 μm. Bigger pad can also be used to increase the capacitance. At this point, the thickness, d, and the associated dielectric constant of the dielectric material become important. In the fabrication, Si_3N_4 (silicon nitride) film and BCB were used as the dielectric material where the dilectric constants of Si_3N_4 film and BCB are between 6-9 and 2.5-2.75, respectively [2, 32, 30]. Therefore, different thicknesses and area sizes were employed during fabrication of capacitance. For BCB layer, approximate sizes were d=8 μm, $\sqrt{A}$ =750 μm and $\epsilon_{BCB} = 2.7$, from which capacitance becomes $C = \epsilon_0 \epsilon_r \frac{A}{d} = 1.68$ pF. For Si_3N_4 film, d=1.5 μm, $\sqrt{A}$ =175 μm and $C = \epsilon_0 \epsilon_r \frac{A}{d} = 1.37$ pF for $\epsilon_r = 7.6$. Finally, the resonance frequncy can be found as, $\omega_0 = 4.5$ GHz for the values of $L = 0.9$ nH and $C = 1.4$ pF.

4.3 Fabrication Processes

In section 4.1, evolution of the device is discussed. There were considerable variations in the final and initial structures which cause corresponding changes in the fabrication processes also. Some parts of the structure were already designed before fabrication processes, such as KOH etching and metal deposition, while some parts had to be changed due to troubles that were encountered during fabrication such as bonding of wire to top surface. In this section, description of the processes that we employed during fabrication are presented. A process, usually, can be realized by utilizing different techniques. Reasons of why a specific technique was chosen for a particular process and, advantages and disadvantages of that technique compared to others are given including associated results. The section begins with describing etching process of silicon and continues with other processes by following the same order of fabrication steps.

4.3.1 Etching of Silicon and Masking

A cavity inside a bulk silicon can be constructed by selectively removing significant amount of silicon from substrate. The most common bulk silicon etchants are TMAH (tetramethyl ammonium hydroxide), EDP (ethylenediamine-pyrocatechol) and KOH (potassium hydroxide)[33]. All these etchants are orientation-dependent, (often called anisotropic), meaning that etchants etch much faster in one direction than in another, revealing the slowest etching crystal planes over time[28]. In the literature, several reasons of anisotropic behaviour are presented. In [25], one of the most important reason is given as the atomic lattice packing density and available bonds in the crystallographic structures of silicon. (111) plane exhibit very high atomic packing density compared to (110) and (100) planes. Therefore, etch rate in the $\langle 111 \rangle$ direction considerably very low compared to etch rates in the $\langle 110 \rangle$ and $\langle 100 \rangle$

directions. Furthermore, the atomic packing density of (110) plane is less dense than that of (100) plane which results in higher etch rate in the ⟨110⟩ direction. On the other hand, in [28], another reason of this anisotropy is specified as screening of the surface by attached H_2O molecules, which is determined by crystal orientation. Another approach can be found in [34, 1]. (110) surface has a more uneven atomic structure than the (100) and (111) surfaces. (111) is tightly packed and has only one dangling bond while the other three bonds remaining in the crystal. The atoms on the (100) plane have two dangling bonds while the other two bound to the crystal. The importance of the dangling bonds is the following: during etching process, hydroxide ions in the etchants, such as OH^- in KOH, can attach to the dangling bonds of an atom and weaken the other bonds that are in the crystal. Therefore, it becomes easy to break an atom from the surface. Since there are two dangling bonds per atom in the (100) plane, it is etched faster.

Comparison of Bulk Silicon Etchants

Anisotropic etching of silicon forms a basis for the resonator structure. It was important to realize a cavity at first. Therefore, in this thesis, most convenient method was preferred to etch the substrate. The choice of etching solution depends on many factors, such as etching rate, anisotropy, cost, selectivity of silicon compared to masking film and surface roughness. In this manner, among the many kinds of etchants, solution of KOH and H_2O was employed during fabrication. One of the other candidates was EDP. EDP (also referred as EPW for ethylene diamine, pyrochatechol and water [35]) is classic but very hazardous and corrosive, and also, its vapor is carcinogenic, therefore it is hard to deal with [28, 36]. On the other hand, TMAH is easy to use and has many advantages. It allows utilizing SiO_2 as an etchant mask and etching of silicon after CMOS fabrication [37, 28]. However, TMAH is expensive compared to KOH[37]. KOH is an

alkali hyroxide etchant used in silicon bulk etching. The key advantages of KOH are low-cost, safe, repeatability and uniformity which allows batch fabrication . However, there are drawbacks of using KOH also. Main drawback is the creation of H_2 gas bubbles during etching. As a result of redox reaction, formation of H_2 gas bubbles onto the surface of the substrate occur [34]. The redox reaction of KOH etching of silicon is given as [28]

$$\mathrm{Si}+2\mathrm{OH}^- \longrightarrow \mathrm{Si(OH)}_2^{++} + 4\mathrm{e}^-$$

$$\mathrm{Si(OH)}_2^{++} + 4\mathrm{e}^- + 4\mathrm{H_2O} \longrightarrow \mathrm{Si(OH)}_6^{--} + 2\mathrm{H_2}.$$

First the oxidation takes place. Silicon bonds are broken and the silicon is oxidized which results in accumulation of four electrons from each silicon atom into the solution. Then, water is reduced and leading to the formation of H_2 gas molecules. The size of the H_2 bubbles and the duration they remain onto the substrate surface depend on the KOH concentration and temperature of the solution. Longer duration of existance of large bubbles onto the surface can stop etching and act as a pseudomask, which increases the surface roughness [38, 34, 39, 29, 40]. The followings can also be considered as other two drawbacks of using KOH: It etches aluminium and therefore, is not compatible with the CMOS devices; and the problem of convex corner undercutting of (100) silicon in KOH can be quite serious [41]. Surface roughness and corner undercutting problems can be avoided by utilizing appropriate techniques. In particular, as KOH concentration and temperature are increased, the diameter of the bubbles produced decreases. Small bubbles leave the surface much faster and KOH can etch the surface. The small bubbles, therefore, cause less rough surface compared to large bubbles [42]. The surface tension of the KOH solution is, also, important for the surface roughness. The surface tension arises from the polar nature of the molecules. For any liquid, lower surface tension means better wetting capability and high degree of attraction with which it has contact. Surface tension of water can be reduced significantly by increasing temperature. In the literature, it is also well known that isopropyl alcohol (IPA) is used in KOH and TMAH solutions

to improve the surface smoothness by decreasing surface tension[40, 43, 44, 37]. Mechanical stirring and megasonic sound will remove the hydrogen bubbles from the surface also. Further improvements can be found in [45]. The other drawback, convex corner udercutting can be avoided by using corner compensation techniques. There are many different compensation techniques. Some of them can be found in [46, 47, 48, 35, 49, 50, 51]. Since, in our case, there are no convex corners and the surface roughness is not a very critical problem as long as the electrical conductivity between the cavity walls is achieved after metal deposition, KOH was a good choice to be used in the fabrication.

KOH Concentration and Temperature

In the previous discussion, it is mentioned that the surface roughness of the etched areas depends on the KOH concentration and the temperature of the solution. However, in addition to the surface roughness, the concentration and the temperature play a key role on the etch rates of the different crystallographic planes. There are many presented work about the KOH etch rates for different concentrations and temperatures [52, 26, 38, 53, 54]. Table 4.1 shows etching rates along various crystallographic directions of Si for KOH concentrations of 30%, 40% and 50% at 70°C. Table 4.1 is reproduced from [1]. In the table, etch rates are given in μm min^{-1} and the numbers in parantheses are the normalized etch rates relative to (110) plane. It can be seen that as the concentration increases from 30% to 40% and 50%, etching rates decrease for the same temperature (except the etch rate of (111) plane which is already very low compared to other planes). Increasing temperature of the solution significantly speeds up the etching rates [54, 42]. In the fabrication, we used KOH concentrations of 23.4 wt% solution which was obtained by 120 gr KOH pellets and 330 gr distilled water at 88°C. The solution was aggressively agitated by spinning a magnet at a

Crystallographic Orientation	**Rates at different KOH Concentration**		
	30%	40%	50%
(100)	0.797 (0.548)	0.599 (0.463)	0.539 (0.619)
(110)	1.455 (1.000)	1.294 (1.000)	0.870 (1.000)
(210)	1.561 (1.072)	1.233 (0.953)	0.959 (1.103)
(211)	1.319 (0.906)	0.950 (0.734)	0.621 (0.714)
(221)	0.714 (0.491)	0.544 (0.420)	0.322 (0.371)
(310)	1.456 (1.000)	1.088 (0.841)	0.757 (0.871)
(311)	1.436 (0.987)	1.067 (0.824)	0.746 (0.858)
(320)	1.543 (1.060)	1.287 (0.995)	1.013 (1.165)
(331)	1.160 (0.797)	0.800 (0.619)	0.489 (0.563)
(530)	1.556 (1.069)	1.280 (0.989)	1.033 (1.188)
(540)	1.512 (1.039)	1.287 (0.994)	0.914 (1.051)
(111)	0.005 (0.004)	0.009 (0.007)	0.009 (0.010)

Table 4.1: Etch Rates of silicon crystallographic planes for different KOH concentrations at 70°C. Reproduced from [1].

rate of 500 rpm. 400-450 μm substrate was etched using this solution in approximately six hours. Notice that this solution is about 23% KOH by weight since the KOH pellets normally contain 10 to 15% water [41]. As stated before, the addition of IPA to the solution improves the surface uniformity which reduces the requirement for stirring. However, the boiling point of IPA is 82°C [55] which is below the solution temperature and it is not very convenient to add IPA to 88°C solution. Isopropyl alcohol also reduces the etching of (110) considerably (in [56] it is given that by 90%) and (100) plane slightly but accelerates the etching of (111) plane [41].

KOH Masking

In a silicon bulk micromachining process, depending on the choice of etchants, silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) film layers are commonly used as an etch mask. In KOH etching, deposition of thin film Si_3N_4 is adequate onto the substrate. Although SiO_2 is also less selective compared to silicon, etching of SiO_2 becomes observable especially in deep etching processes. Deposition of Si_3N_4 on a Si substrate is typically made by either using PECVD or LPCVD techniques. It is known that PECVD nitride is less selective compared to LPCVD nitride [32]. The etching rates of Si_3N_4 made by LPCVD and PECVD are given in [57] as 10 Å/hr and 400 Å/hr for 30% KOH at 70°C, respectively. PECVD nitride has many pinholes and is not very suitable as an etch mask for removing 400-450 μm silicon substrate. Futher comparison of LCPVD and PECVD Si_3N_4 can be found in [32, 41].

The first step of the fabrication was deposition of LPCVD Si_3N_4 film onto the 500 μm thick, SSP (single side polished), (100) silicon wafers. This process was done in TÜBİTAK YİTAL Laboratories at Gebze. A stoichiometric nitride film was deposited onto the both sides of the wafer, at 800°C. A film thickness was 50 nm, which is pretty sufficient to etch the substrate 400 μm deep. A thicker film causes additional tensile stress on the wafer. There are also techniques to realize low stress (silicon-rich) LPCVD nitride films for reducing the stress while keeping the same KOH etch rate [58].

Here, it is worthwhile to mention that DSP (double side polished) wafers would be more appropriate for the fabrication rather than SSP wafers. The problem was not the deposition of Si_3N_4 films onto unpolished surface but, as discussed in the following sections, was in the processes of standard photoresist spinning and lithography, and, especially, in metal deposition, in which loss due to the surface roughness is increased. It is hard to employ these processes to such unpolished surfaces. As a summary, if we emphasize again, LPCVD Si_3N_4

film onto both sides of the SSP wafer was successfully deposited and used as a mask in the fabrication steps followed.

4.3.2 Lithography and Mask Design

After deposition of Si_3N_4 films, the wafers were diced into 1 cm x 1 cm individual pieces in METU MET Laboratories using a die saw. Then, lithography was done at the Bilkent University Advanced Research Labs. The substrate of some of these dies were removed completely to realize the upper half of the cavity shown in Figure 4.5, while the lower half was etched about 400 μm. Therefore, during lithography processes different mask patterns were employed for these two cases. After standard photoresist spinning and lithography, the Si_3N_4 films at the exposed regions were selectively removed by RIE (reactive ion etching). For RIE etching of Si_3N_4, PR acts as a mask. The PR spin and RIE etch processes, in this step, were employed to the unpolished side. Polished side was kept for capacitor fabrication where surface roughness is more serious.

In section 4.2, the width of the openning, w, in Figure 4.5, is given as 650 μm. The required width in the mask pattern can be calculated from Figure 4.6(a)

$$w\_mask = w + 2\frac{500\ \mu\text{m}}{\tan 54.74} \tag{4.3}$$

$$= 1350\ \mu\text{m}. \tag{4.4}$$

Therefore, in order to achieve 650 μm wide opening at the other side of the substrates after KOH etching, 1350 μm wide Si_3N_4 must be removed from the top surface. The substrates were left into the KOH solution for about 1.5 hours leading to 100 μm substrate etching. Then, another lithography and RIE processes were employed to remove Si_3N_4 from regions that remain inside the cavity. By this way, cavity volume can be increased. Figure 4.7(a) shows this step. Note that, the thickness of Si_3N_4 in Figures 4.7 and 4.6 is only 50 nm and, for convenience, is drawn in oversize compared to substrate. In Figure 4.7(c), the di-

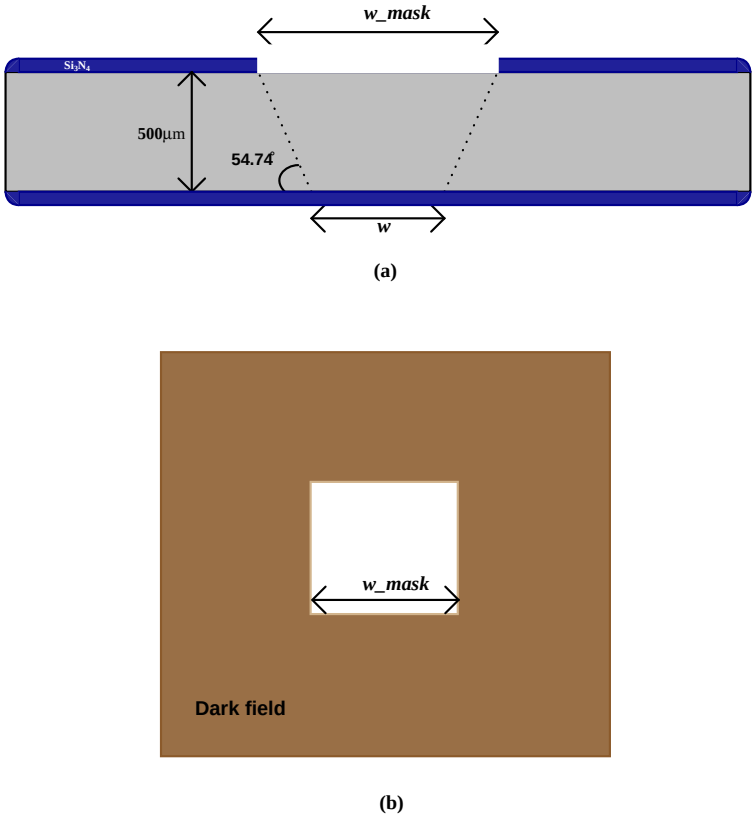


Figure 4.6: (a)Removal of Si_3N_4 before KOH etching. (b)Corresponding mask pattern.

mensions of the mask pattern for this process is shown. Note that the dimensions are defined in terms of the size of the cavity, $2b$.

4.3.3 Metal Deposition

After KOH etch processes are completed, remaining Si_3N_4 layers were completely removed from both faces by using RIE. And the substrates became ready for metal deposition. This process was done by evaporating metals in a vacuum chamber. The primary intention was evaporating gold (Au) layer to the side walls of the cavity. Gold was chosen, because it can exhibit high resistance to oxidation[59]. Titanium (Ti) was used as an adhesion layer, since inert metals, such as gold, do not adhere well to the silicon substrate. The adhesion layer

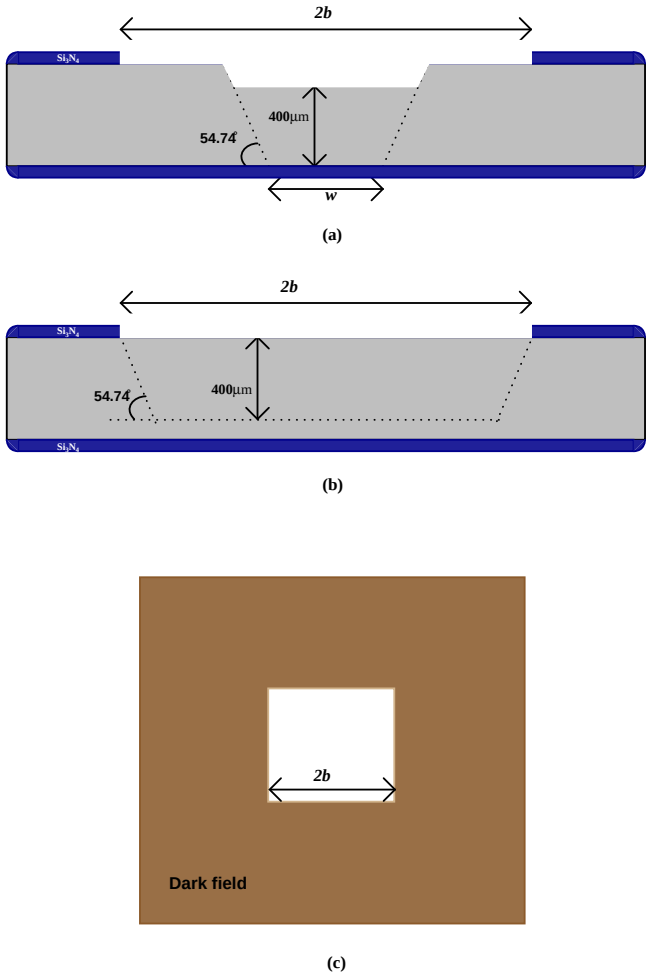


Figure 4.7: Removal of Si_3N_4 in accordance with the desired cavity dimensions. (a) Dies, after 100 μm KOH etching, that make up the upper part, (b) dies that make up the lower part of the resonator. (c) Corresponding mask pattern, used in this step

was depositied about 15 nm without breaking the vacuum. At this step of the fabrication we encountered a problem. After deposition of gold, it was observed that gold film peeled off immediately from the silicon substrate for both polished and unpolished sides. This happened many times and thus instead of gold, aluminium (Al) was used, after this experience, without including an adhesion layer. Aluminium deposited about 2 μm. As the thickness of metal increases, the associated skin loss becomes less. But, deposition of even several microns is not very easy task by evaporation. Electroplating can be used at this point but the conductivity of the metal would be certainly reduced.

4.3.4 MIM Capacitor

The lower half structure of the cavity was completed after aluminium deposition to the etched surface. On the other hand, for the upper part, a capacitor should be fabricated on the polished side of the substrate before bonding two dies together as indicated in the design. The capacitor was fabricated on the polished side, since it is easy to pattern compared to unpolished side and to reduce the associated losses. During fabrication, PECVD Si_3N_4 and BCB based CYCLOTENE were coated on the aluminium surface as a dielectric material of the capacitor. BCB is a spin-on material and, therefore, compared to PECVD Si_3N_4, deposition process is much easier. However, it requires curing step at 300 °C, about 2 hours. For a spin rate of 5000 rpm, the thickness of the BCB material after curing was measured as 8 μm. Next step was, removing the BCB from the surface regions that remain out of the pad area as shown in Figure 4.8. RIE etching receipe of CYCLOTENE is given in [60]. Pressure of 250 mTorr, at 100 W RF-power, O_2 and CF_4 flow rates of 90 sccm and 10 sccm, respectively, result in an etch rate of 0.6 μm/min. But, in the fabrication, we could not etch the BCB polymer because of lack of CF_4 in the lab. Nevertheless, the capacitor was done without removing BCB from the surface. Aluminium was deposited again, but this time onto the BCB polymer and the pad was brought out after lift-off process. The construction of capacitor is shown in Figure 4.8(d). The measuremnt of this capacitor is given in chapter 5.

Si_3N_4 was also tested as a dielectric material of the capacitor. First, PECVD nitride was deposited at 250°C. In [32], it is given that good quality PECVD Si_3N_4 films can be obtained for temperatures higher than 300 °C. The thickness of the nitride film was around 1.2 μm. Note that, it is possible to deposit thicker nitride films by using PECVD compared to LPCVD, since the PECVD nitride has relatively low residual stress[53, 61]. Then, image reversal photoresist was employed and Si_3N_4 was removed from regions outside the pad area by RIE.

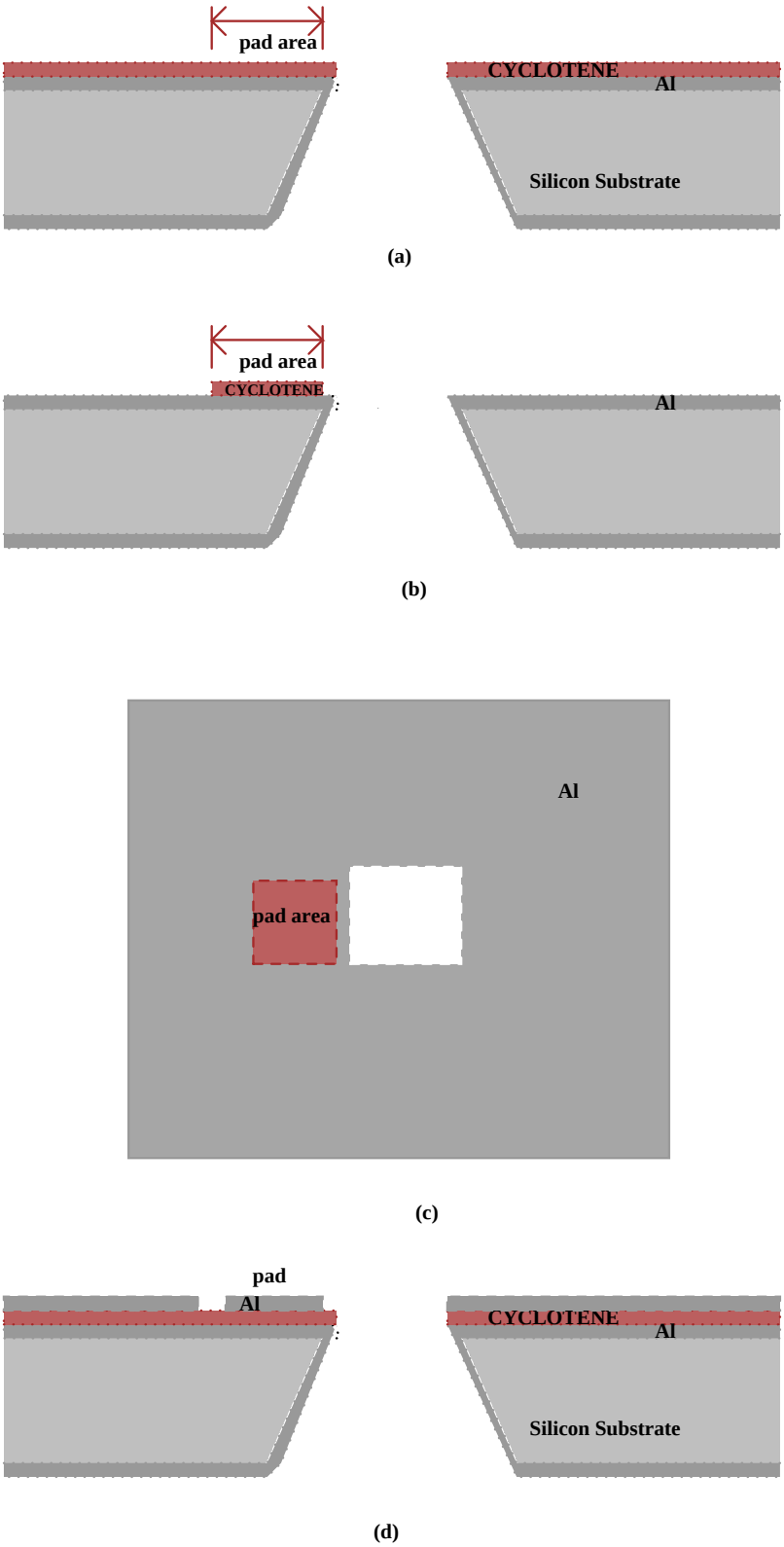


Figure 4.8: (a) Deposition of BCB over Al. (b) Etching of BCB. Side view. (c) Top view. (d) Construction of MIM BCB Capacitor

Another photoresist and lithography processes followed to define lift-off regions. The mask patterns used in these steps are shown in Figure 4.9. Lift-off pattern is simply a frame between the signal and the ground pads. Note that, the size of the signal pad area equals to the area of the upper electrode of the capacitor. After aluminium deposition, metal must be completely lifted-off from the these regions. To achieve this, photoresist under aluminium should be removed by acetone. Lift-off processes can be sped up by heating the acetone or by placing it into an ultrasonic tank[41]. If a very thick metal is deposited at this step, this will impede the touch between acetone and photoresist regions, which results in unsuccessful lift-off patterning. Therefore, at this step of the fabrication, the thickness of metal was set to 1.2 μm. As stated before, loss due to the skin effect can be reduced by depositing thicker metals. The removal of photoresist under the thick metal can be realized if a special lift-off resist (LOR) is coated. The fabrication of the capacitor was completed at this point.

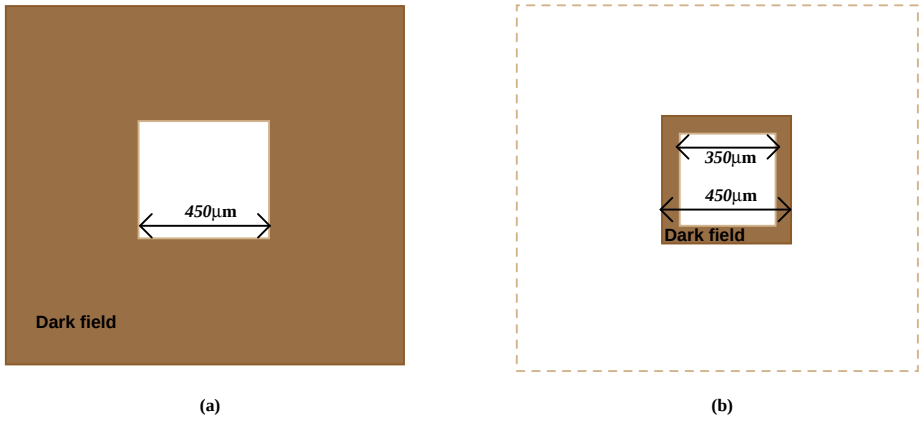


Figure 4.9: Mask patterns. (a) Image is reversed for this pattern to select Si_3N_4 region under pad. (b) Pattern defines the lift-off regions

4.3.5 Epoxy and Ball Bonding

At this step of the fabrication, the upper and lower part were brought together and bonded by silver epoxy. Silver epoxy acts as a glue which offers electrical conductivity. However, it certainly causes some loss due to the contaminants it contains. Therefore, epoxy film was coated between the dies as thin as possible. Then, it was cured at 120 °C for about 15 minutes. By employing thermcompression bonding of dies, the loss due to the epoxy can be avoided.

To make a wire bonding inside the cavity as shown in Figure 4.5, Kulicke and Soffa ball bonder was used. The radius of the wire was 25 μm. Thicker wires tend to increase the quality factor of the resonator since the RF resistance of the wire increases inversely with the wire thickness, hence decreasing the Q of the inductor. One of the best options for this process is, using ribbon wire instead of round wire. There are many advantages of using ribbon wire as given in [62]. Ribbon wire offers larger cross-section at the heel of the bond so there is more surface contact which provides better connection and higher reliability. Current carrying ability is also much better than round wire of same length leading to the reduction of loss due to skin effect. Deep access ribbon wire bonding tool is available in the market [31].

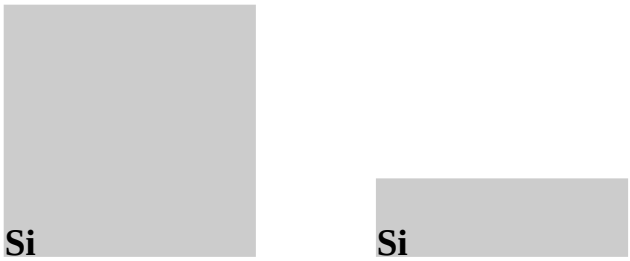
Last step of the fabrication was ball bonding. The first bonding was done at the base of the cavity as shown in Figure 4.5 and the second bond was intented at the outside pad, which is the top electrode of the MIM capacitor. However, it was observed that the force applied by the bonder to make a succesful bonding, was enough to short-circuit the capacitor electrodes and destroy it. Thus, the second bonding was done using silver epoxy under microscope. Epoxy and ball bonding processes were accomplished in METU MEMS Lab.

After the fabrication was completed, the measurements were done in Bilkent University Microwave Lab. using Hewlett Packard Vector Network Analyzer.

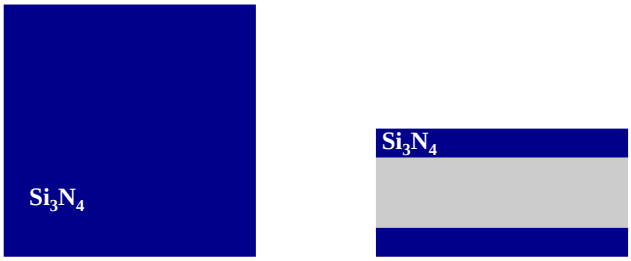
4.4 Process Flow

In this section, the graphical representation of each fabrication step is presented for both upper and lower half structures.

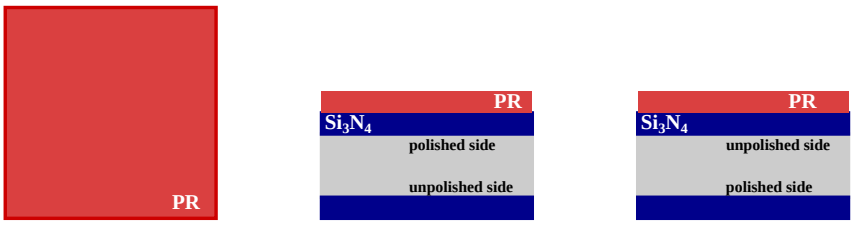
1. Starting point, bare SSP silicon



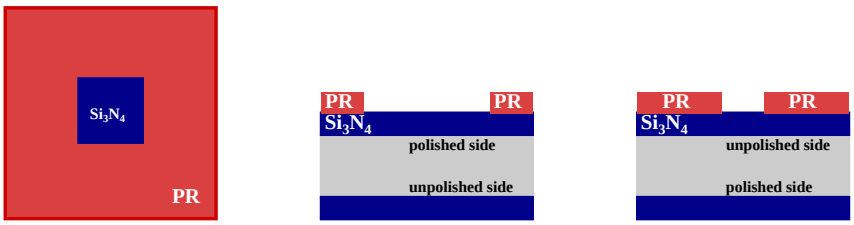
2. LPCVD silicon nitirde deposition



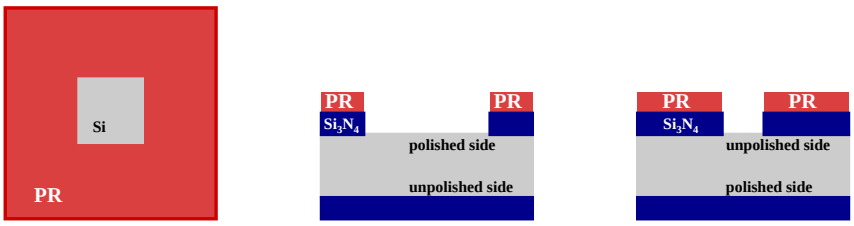
3. PR spin on unpolished and polished sides for upper and lower half structures respectively



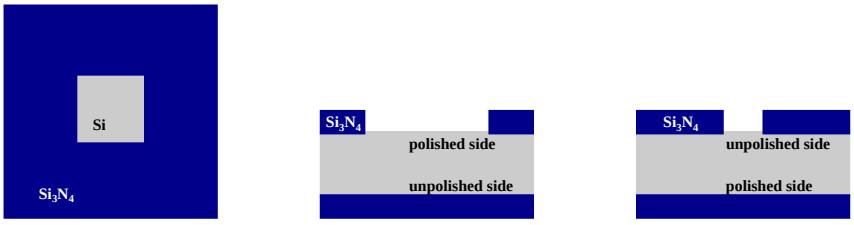
4. Pattern PR



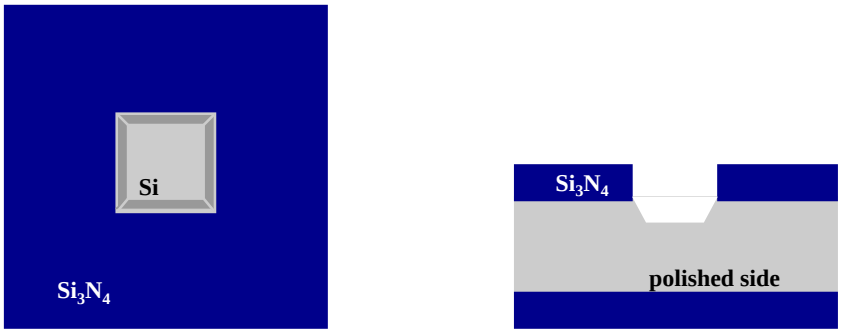
5. RIE etch of Si_3N_4



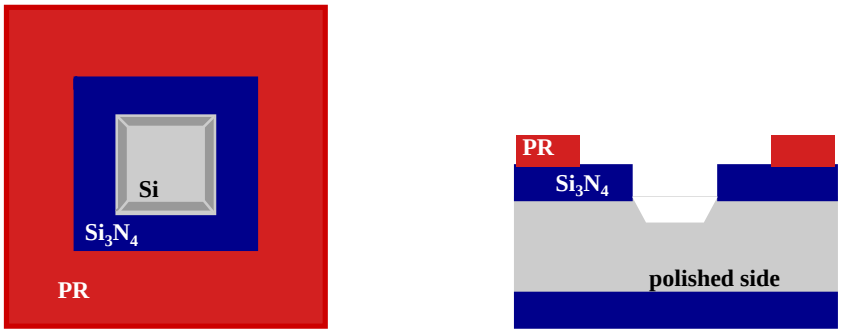
6. Remove PR



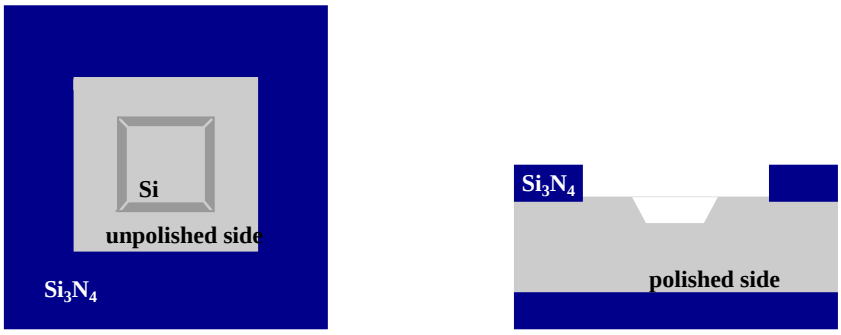
7. 100μm KOH etching



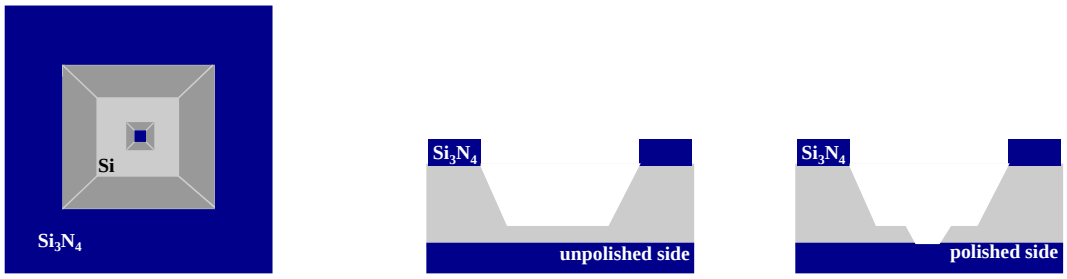
8. Spin and pattern PR



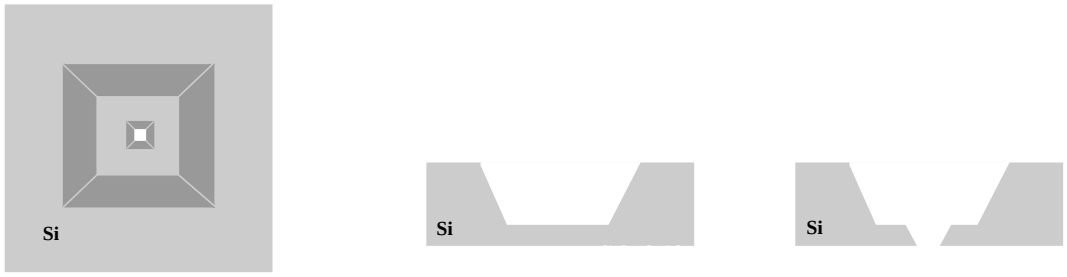
9. Remove PR and RIE etch of Si_3N_4



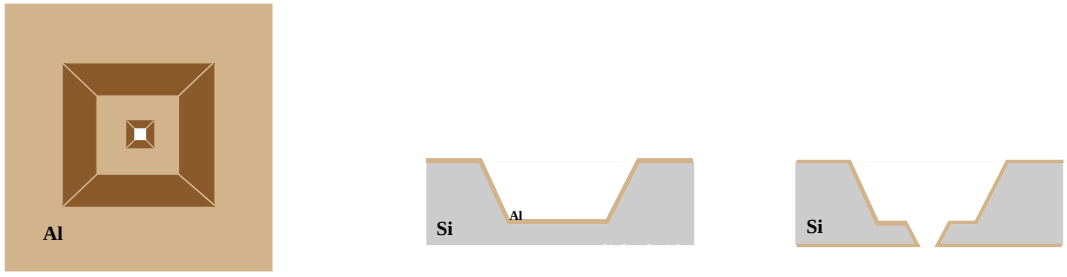
10. 400μm KOH etching



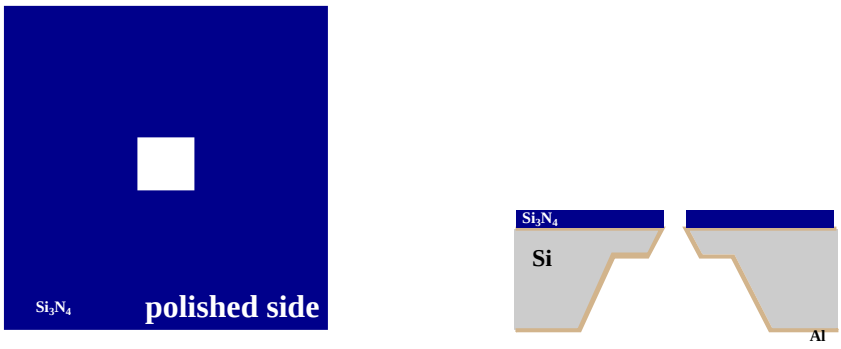
11. RIE etch of Si_3N_4 from both sides



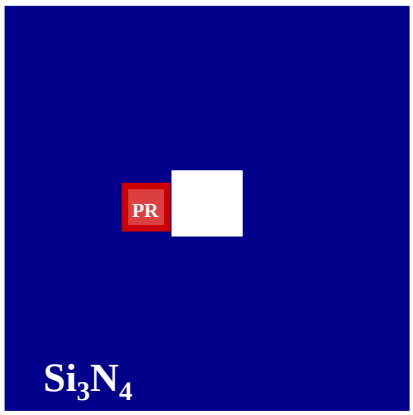
12. Aluminium Deposition

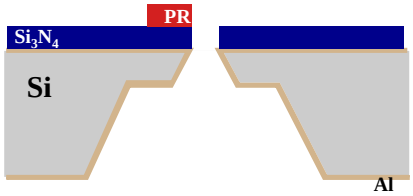


13. PECVD Si_3N_4 deposition onto the polished side

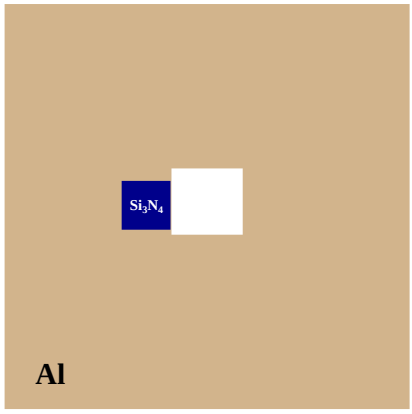


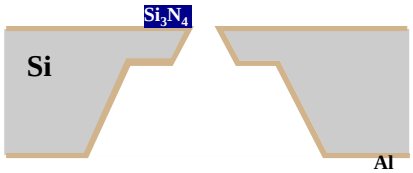
14. Spin and pattern PR



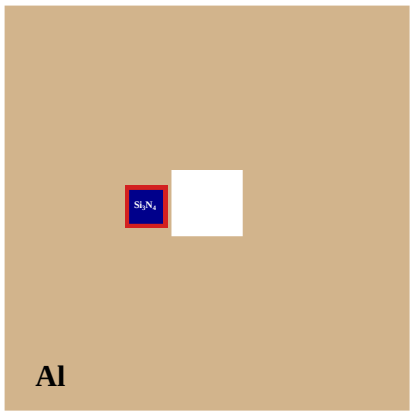


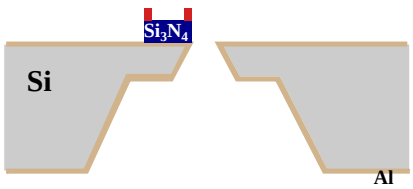
15. RIE etch of Si_3N_4 and remove PR



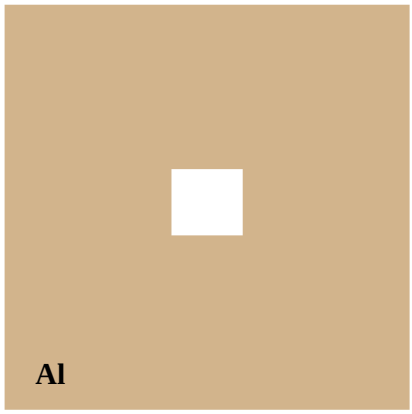


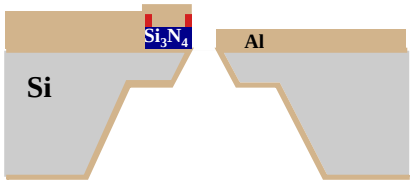
16. Pattern lift-off regions



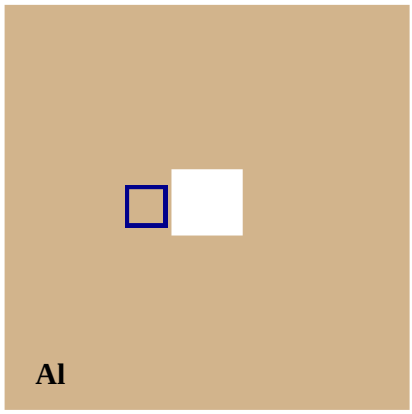


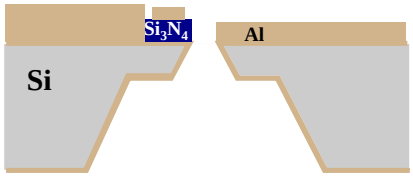
17. Aluminium deposition



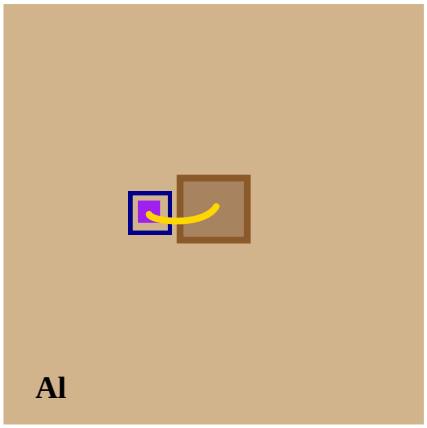


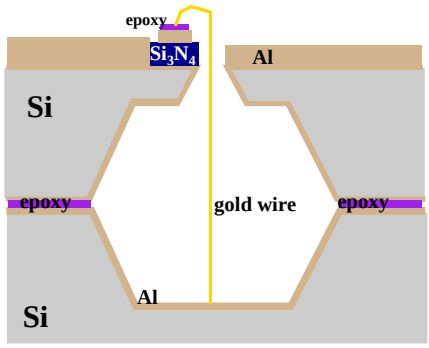
18. Lift-off





19. Epoxy and wire bonding





Chapter 5

MEASUREMENTS OF THE ON-CHIP RESONATOR

The measurements of intermediate steps and device that were carried out during and after fabrication, are presented in this chapter. Intermediate measurement steps include KOH etching, metal deposition, PECVD nitride and capacitor. When all processes accomplished, the resonator structure was measured finally.

After first 100 μm KOH etching, the etch depth was measured using optical microscope. The depth of etch is not very critical for the device; a depth of 150 μm would also be acceptable. Therefore, the measurements were carried out by visually inspecting under a microscope. The fotographs of KOH-etched silicon substrates are given in Figures 5.1, 5.2 and 5.3.

Both sides of the KOH-etched substrate were coated with aluminium by thermal evaporation. Dektak Profilometer tool was used to measure the thickness of the deposited metal film. During measurements, it was observed that metal deposition is not very uniform at the unpolished surface due to the rough surface. The thickness of the metal deposited at the polished surfaces were measured as 2 μm and 1.4 μm for the first and second evaporations of Al (step 12 and step 17

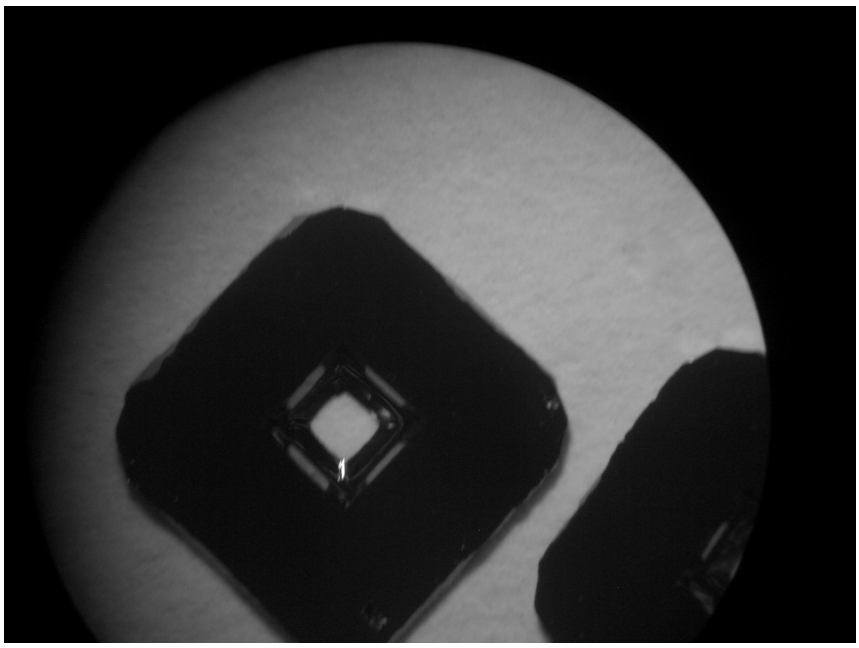


Figure 5.1: Photograph of KOH-etched substrate.

as given in section 4.4), respectively. After both sides were coated with Al, the electrical conductivity between the side walls and between the top and bottom surfaces were confirmed by using a multimeter and a microscope.

Another Dektak measurement was carried out for the thicknesses of the BCB and PECVD nitride films during fabrication of capacitance. The nitride film thickness was measured as 1.2 μm while the thickness of the BCB, which was spinned at 5000 rpm, was measured as 8 μm .

5.1 MIM Capacitor Measurements

Before bonding two dies together and gold wire, the last intermediate measurement step was carried out. MIM capacitor fabricated on the surface was measured. Some photographs from the fabrication of the pad area, lift off regions, and different size capacitors are shown in Figures 5.4, 5.5, 5.6, 5.7 and 5.8. As

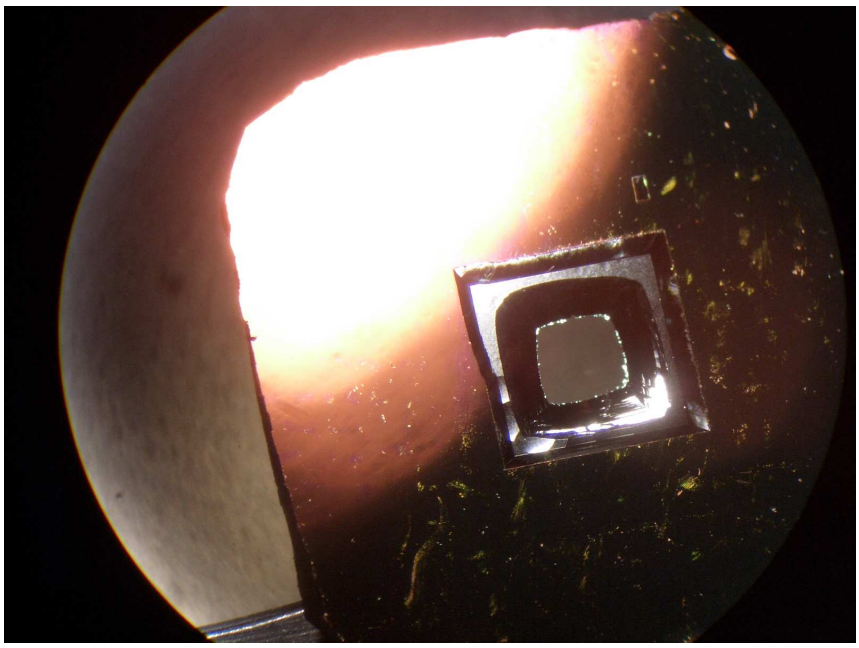


Figure 5.2: Photograph of KOH-etched substrate.

shown in section 4.5, the width of the lift-off regions was set to be around 50 μm. To measure the capacitor under the pad area, 150 μm pitch, two tips (ground-signal) RF probes were connected to HP 8753D Vector Network Analyzer. The calibration was done using these probes under a microscope. Measurements were, also, done under a microscope by contacting the signal tip of the probe with the signal pad and the ground tip with the ground pad. Ground pad is the entire surface of the substrate that remain outside of the signal pad and the lift-off regions.

The smith chart of a BCB dielectric MIM capacitor is shown in figure 5.9. It can be seen that at low frequencies (below 1 GHz), the sketch follow the outermost circle of the chart and, therefore, the device exhibits very low loss. As the frequency increases, the sketch deviates from the circle and bends into the center of the chart. This shows, the loss mechanism inside the capacitor varies with frequency. The same situation can also be seen from Figure 5.10. The capacitance was measured as 1.8 pF. The dielectric constant of BCB material

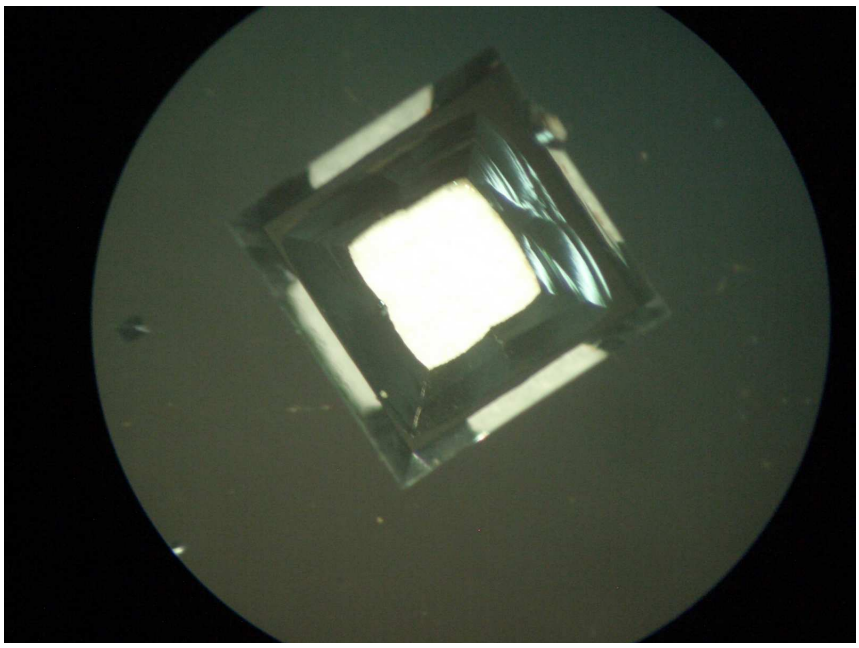


Figure 5.3: Photograph of KOH-etched substrate.

can be calculated using this result. The physical dimensions of the capacitor was,

$$\begin{aligned} A &= 750\ \mu\text{m} * 750\ \mu\text{m} \\ &= 562500\ \mu\text{m}^2 \\ d &= 8\ \mu\text{m} \end{aligned}$$

so the ϵ_{BCB} is computed as

$$\begin{aligned} \epsilon_{BCB} &= C\frac{d}{\epsilon_0 A} \\ &= 2.89. \end{aligned}$$

The quality factor of the capacitor is shown in figure 5.10(d) as a function of frequency. Note that, above 1.5 GHz, Q_C is smaller than 20.

Network analyzer plots of Si_3N_4 dielectric MIM capacitor are shown in Figures 5.11 and 5.12. At a first glance, smith chart plot indicates that the dielectric loss of the capacitor is much smaller in this case, leading to the higher quality

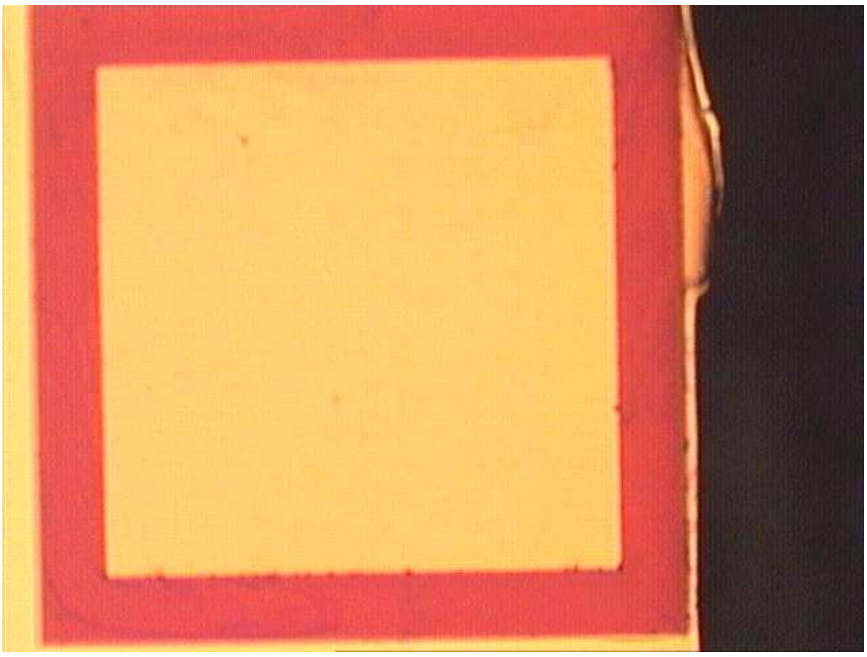


Figure 5.4: Signal pad is enclosed by a frame. Silicon nitride is shown at the lift-off regions

factor. The real and imaginary parts of the admittance between the signal pad and the ground pad are given in Figures 5.12(c) and 5.12(a), respectively. Note that, the imaginary part, ωC_p, is almost a linear function of frequency over a wide band, from 50 kHz to 4 GHz. The associated capacitance value, C_p, is plotted as a function of frequency in figure 5.12(b). At low frequencies, (below 1 GHz), the value of C_p is around 3.8 pF. As the frequency increases, C_p starts to vary in the range from 3.6 to 3.9 pF. However, the variation is small and the value of C_p can be considered as constant over wide range of frequency. The dielectric constant of the deposited Si_3N_4 film can be found using the value of, C_p, the pad area, A, and the thickness of the Si_3N_4 film. For this capacitor,

$$\begin{aligned} A &= 200\ \mu\text{m x } 200\ \mu\text{m} \\ &= 40000\ \mu\text{m}^2 \\ d &= 0.6\ \mu\text{m} \end{aligned}$$

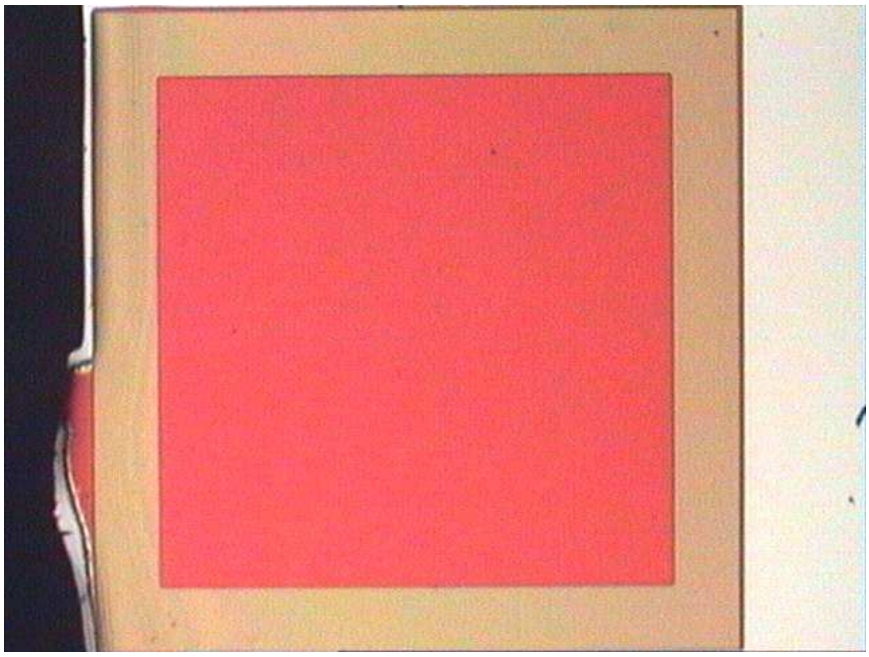


Figure 5.5: Lift-off regions are defined and patterned before metal deposition.

which leads

$$\begin{aligned} \epsilon_{Si_3N_4} &= C\frac{d}{\epsilon_0 A} \\ &= 6.5 \end{aligned}$$

In the following discussions, this result is used as a dielectric constant of Si_3N_4 film. The real part of the admittance shows the conductance between the signal and ground pads. The non-zero conductance causes ohmic losses and reduces the quality factor of the capacitor. The reasons of ohmic losses along this path are parasitic resistance of the dielectric and series resistance of the top electrode of the capacitor. In Figure 5.12(c), the equivalent resistance is denoted by R_p. Note that, the conductance of the parallel path increases with the frequency. The quality factor of the capacitor is shown in figure 5.12(d) as the frequency varies from 500 MHz to 4 GHz. Q_C was measured as around 23-30 between frequencies of 2 and 3 GHz.

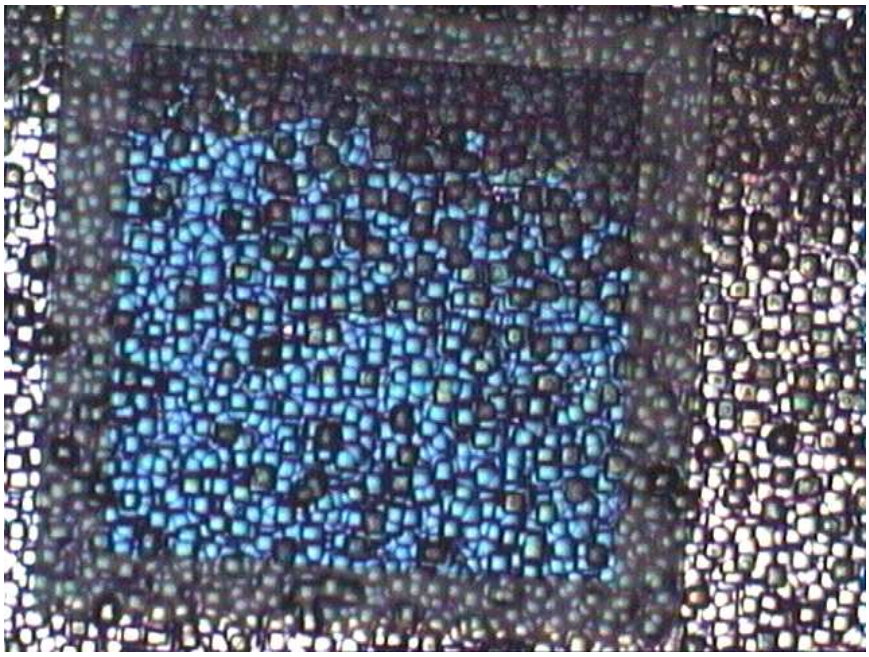


Figure 5.6: Surface roughness of the unpolished side is very poor. It is hard to recognize lift-off regions and the pad area.

5.2 Cavity Resonator Measurements

After epoxy and ball bonding processes completed, the device was measured in the same way as capacitors. The photographs taken during fabrication are shown in Figures 5.13, 5.14, 5.15 and 5.16. And the associated smith chart graph and the impedance of the measured device are given in Figures 5.17, 5.18 and 5.19. The frequency, at which the impedance becomes purely real and reaches its maximum value, is the resonance frequency, f_{res}, and found as 2.78 GHz. For the capacitance value, $C_p = 3.8$ pF, the resonance frequency would be below 2 GHz. Therefore, during fabrication of thre capacitor, the pad area and the Si_3N_4 film thickness were modified to reduce the value of C_p and to increase f_{res}. The dimensions of the capacitor were changed as follows,

$$A = 175\ \mu\text{m x } 175\ \mu\text{m} \quad (5.1)$$

$$= 30625\ \mu\text{m}^2 \quad (5.2)$$

$$d = 1.3\ \mu\text{m} \quad (5.3)$$

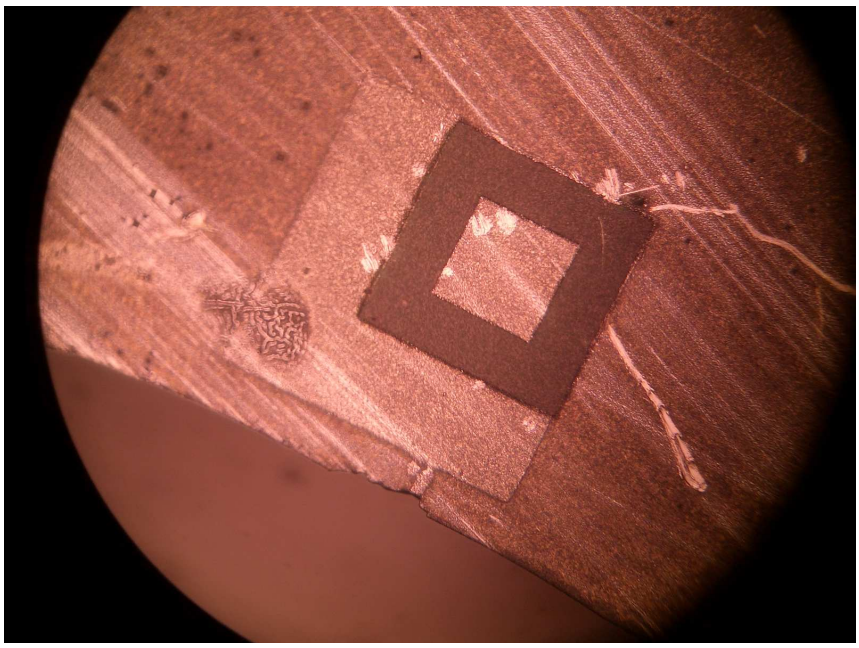


Figure 5.7: Capacitor lies under the signal pad. Note that, lift-off regions are bigger and pad area is smaller compared to 5.4.

$$C = \epsilon_0 \epsilon_{Si_3N_4} \frac{A}{d} \tag{5.4}$$

$$= 1.355 \text{ pF} \tag{5.5}$$

where $\epsilon_{Si_3N_4} = 6.5$ is used. Then, the quality factor at resonance frequency, Q_{res}, can be found from figure 5.18 and directly using equation 2.16.

$$Q_{res} = 2\pi f_{res} C_p R_p \tag{5.6}$$

$$R_p = 1190 \tag{5.7}$$

$$C_p = 1.355 \text{ pF} \tag{5.8}$$

$$Q_{res} = 28 \tag{5.9}$$

The inductance value of the cavity, L, is calculated from equation 2.21.

$$L = \frac{1}{\omega_0^2 C_p} \tag{5.10}$$

$$= 2.42 \text{ nH} \tag{5.11}$$

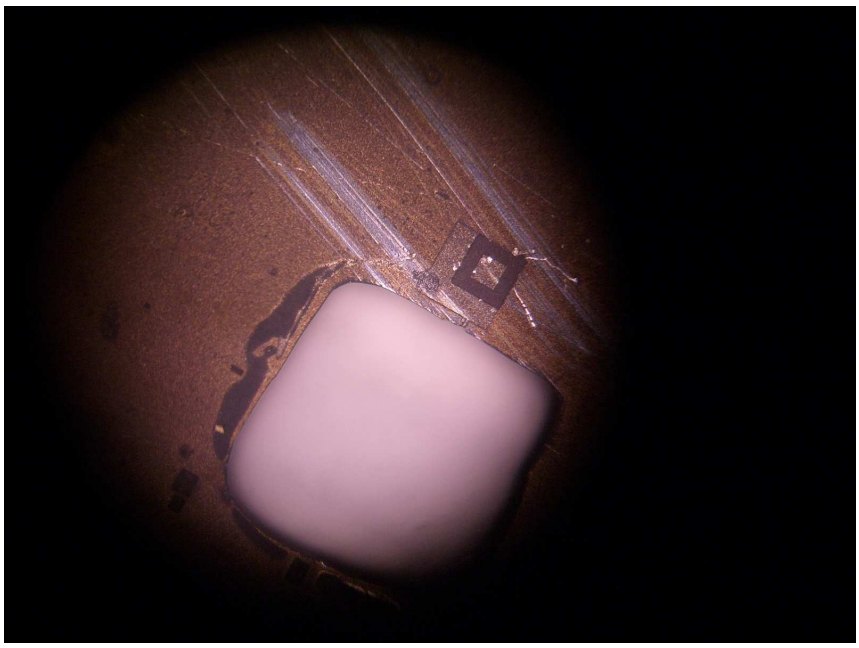


Figure 5.8: Another photograph of the capacitor and the openning.

Note that in equation 2.17, which is repeated here for convenience, Q_{res} is given by in terms of Q_C and Q_L.

$$\frac{1}{Q_{res}} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{5.12}$$

If two of them are known, the third one can be found. The measured Q of the capacitor at the resonance frequency of the resonator is approximately 25 while the theoretically calculated Q of the inductor at the same frequency is 120. The measured Q of the resonator is 28. This seems rather inconsistent but, it also shows that the effect of the Q of the inductor, Q_L, is negligible and the negative difference at the Q measurement can be attributed to the uncertainties of the measurements. Therefore the measurement is consistent with the theory.

Note that, the quality factor of the resonator can also be found from magnitude of the resonator impedance, which is shown in figure 5.20. The resonance frequency is 2.78 GHz, the 3dB cut-off frequencies are 2.715 and 2.814 GHz and

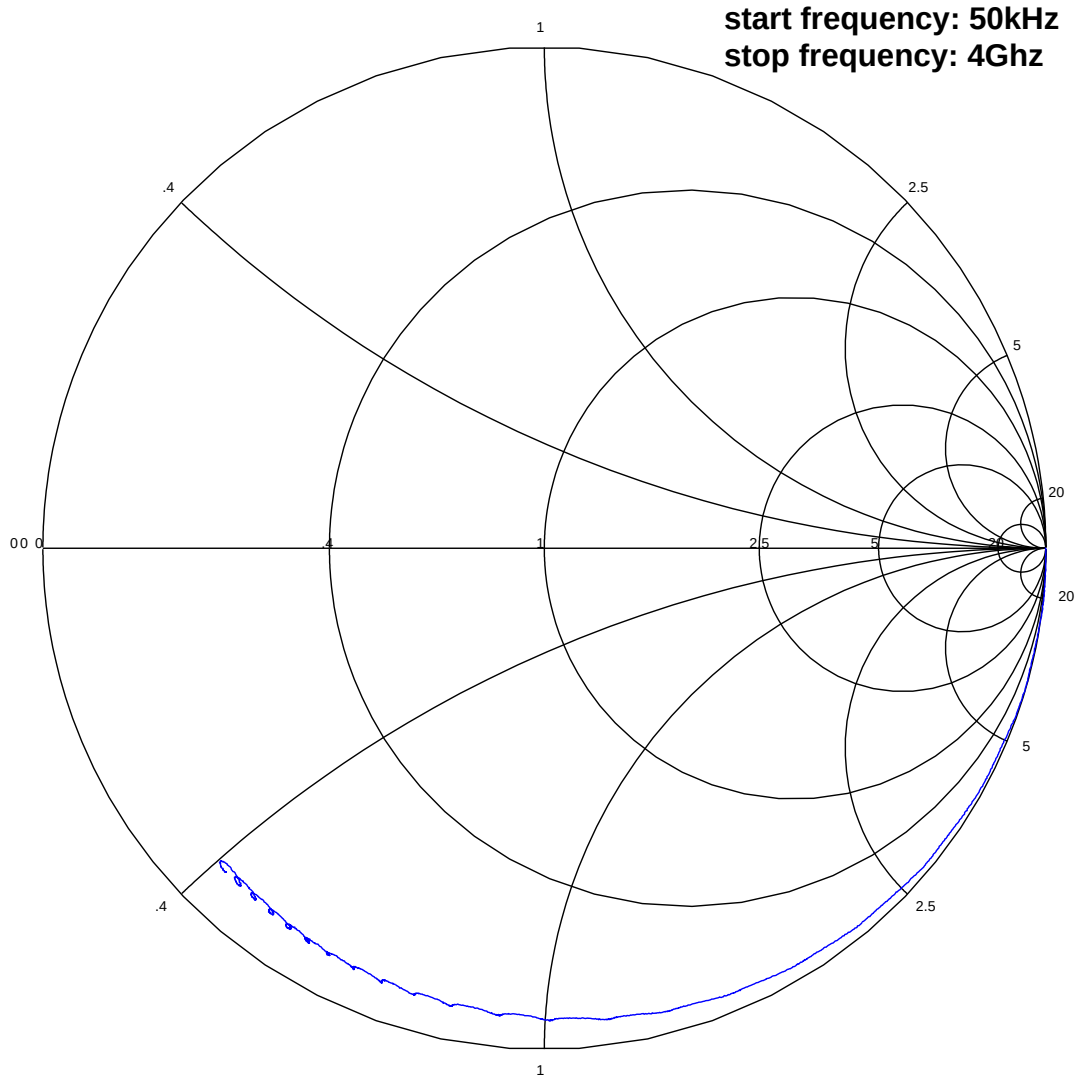


Figure 5.9: Smith chart plot of the capacitor. BCB was used as a dielectric layer.

so that Q_{res} will be,

$$Q_{res} = \frac{f_{res}}{\Delta f} \tag{5.13}$$

$$= \frac{2.78 \text{ GHz}}{99 \text{ MHz}} \tag{5.14}$$

$$= 28.1 \tag{5.15}$$

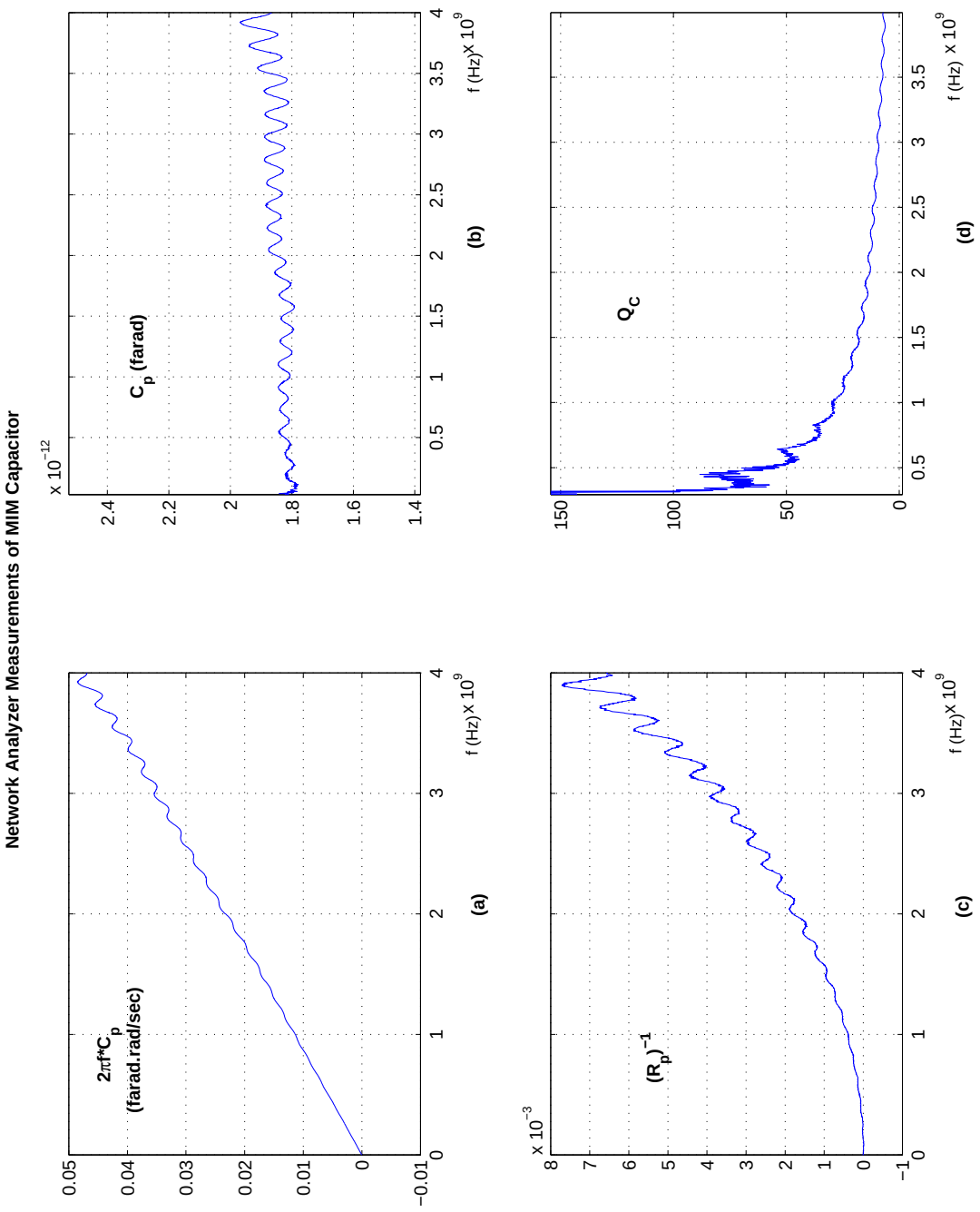


Figure 5.10: Measurements of the BCB capacitor.

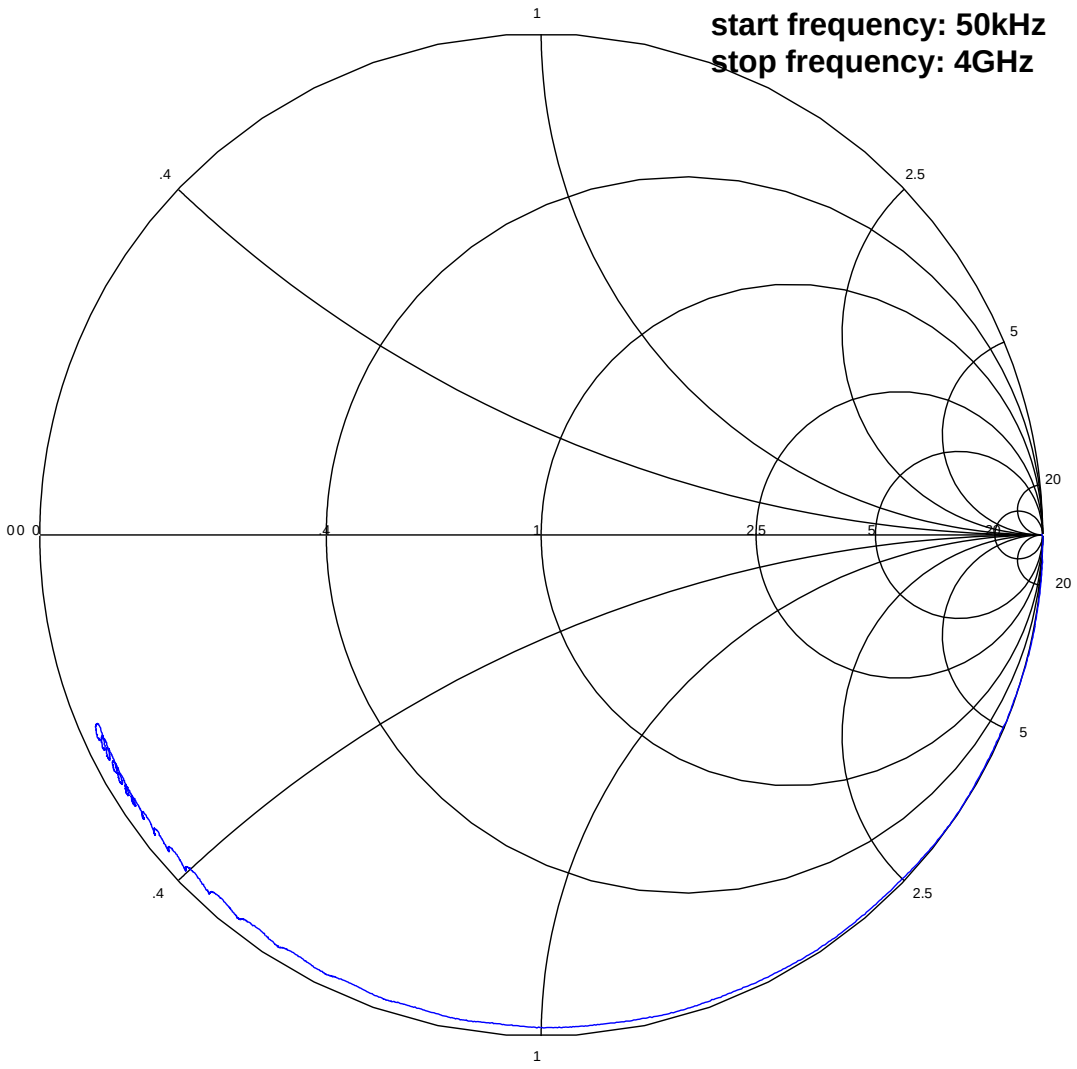


Figure 5.11: Smith chart plot of the capacitor. Si_3N_4 was used as a dielectric.

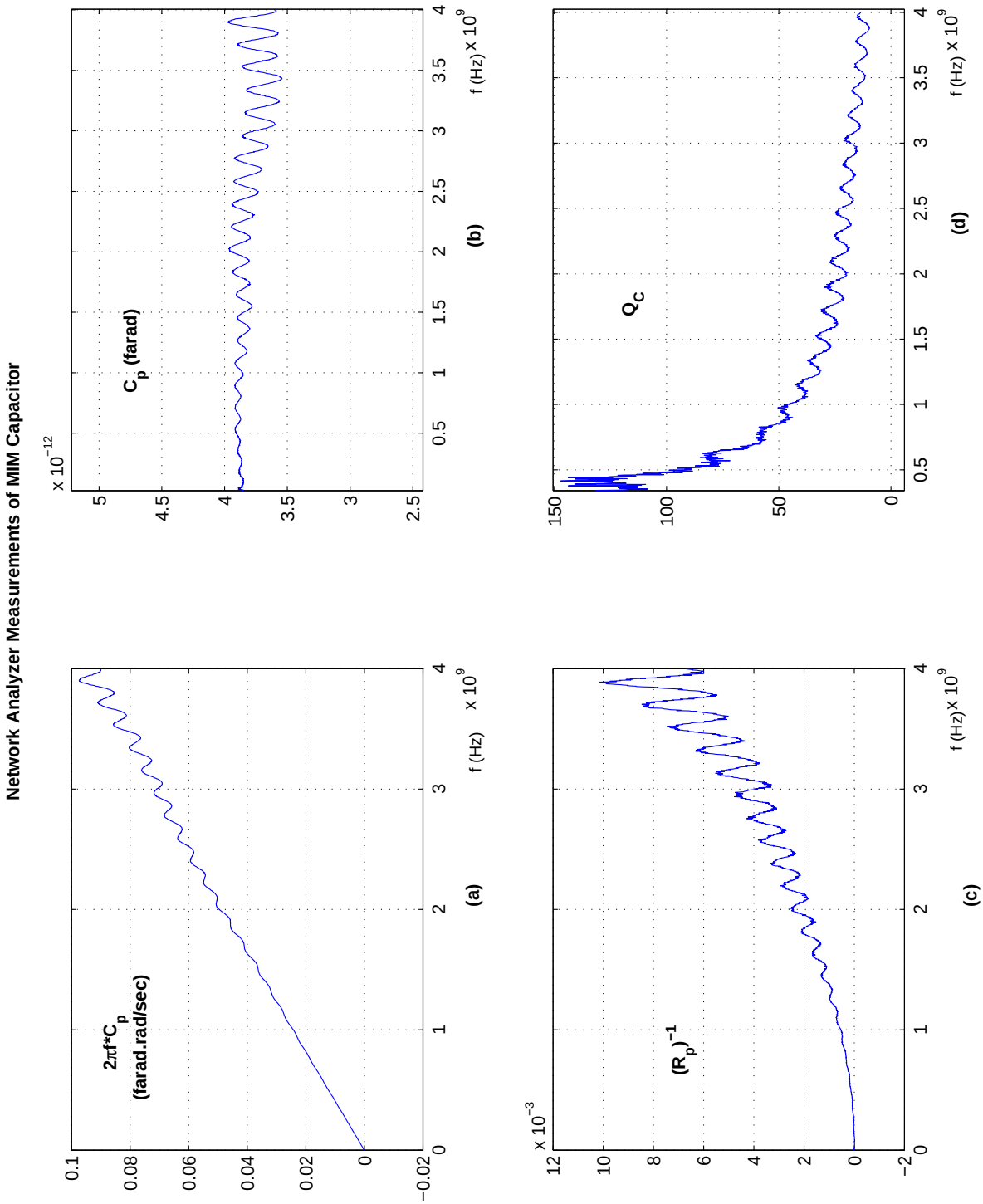


Figure 5.12: Measurements of the Si_3N_4 capacitor.

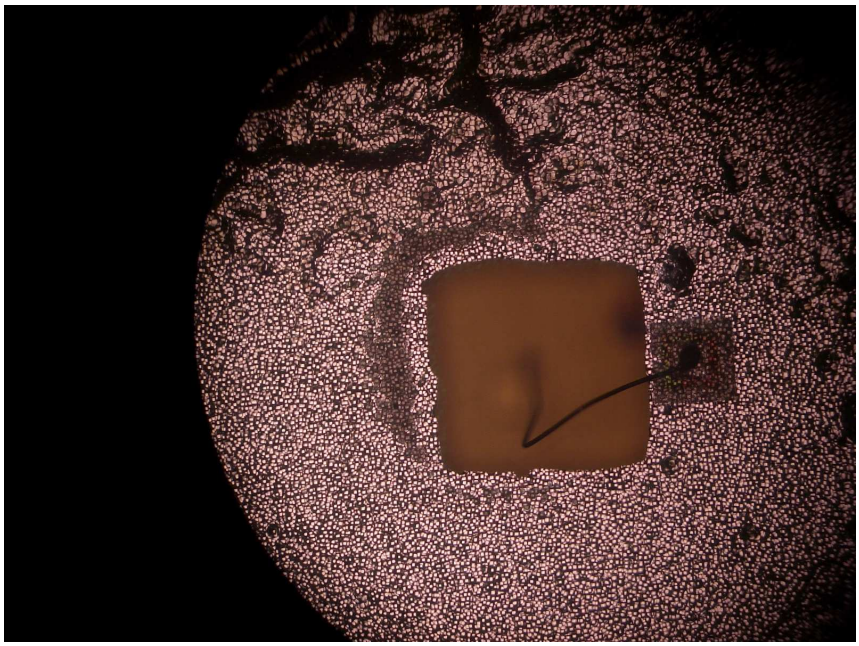


Figure 5.13: Ball bonding process.

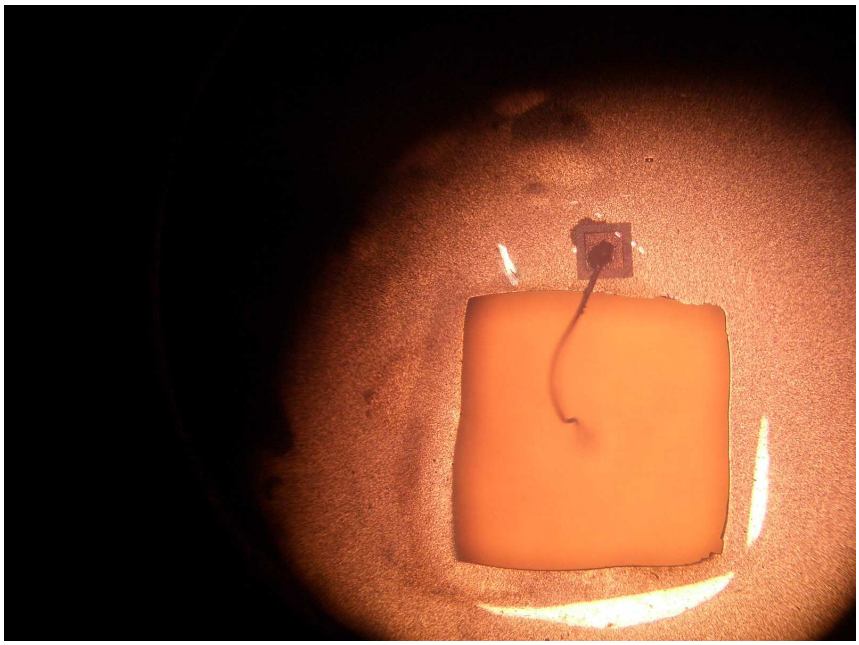


Figure 5.14: Note that the wire has a contact only with the pad and the lower substrate.

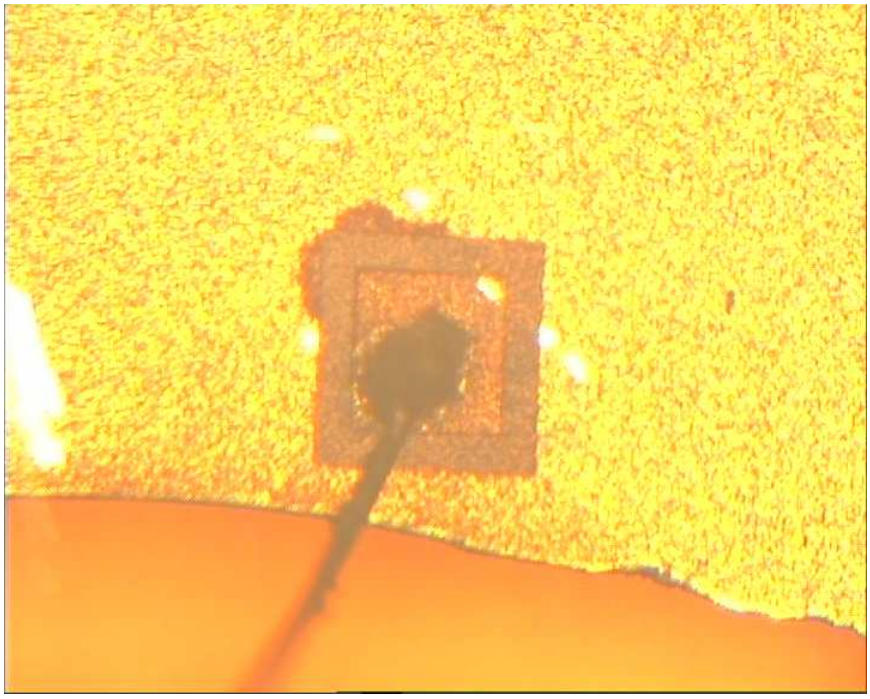


Figure 5.15: Another photograph of the cavity resonator.

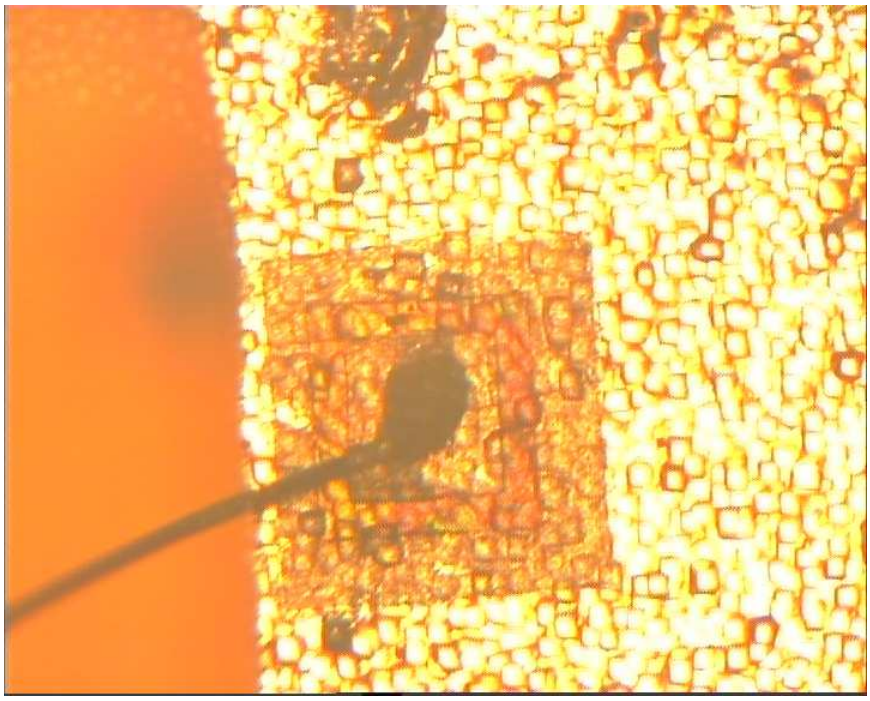


Figure 5.16: Photograph taken during ball bonding process for the unpolished surface.

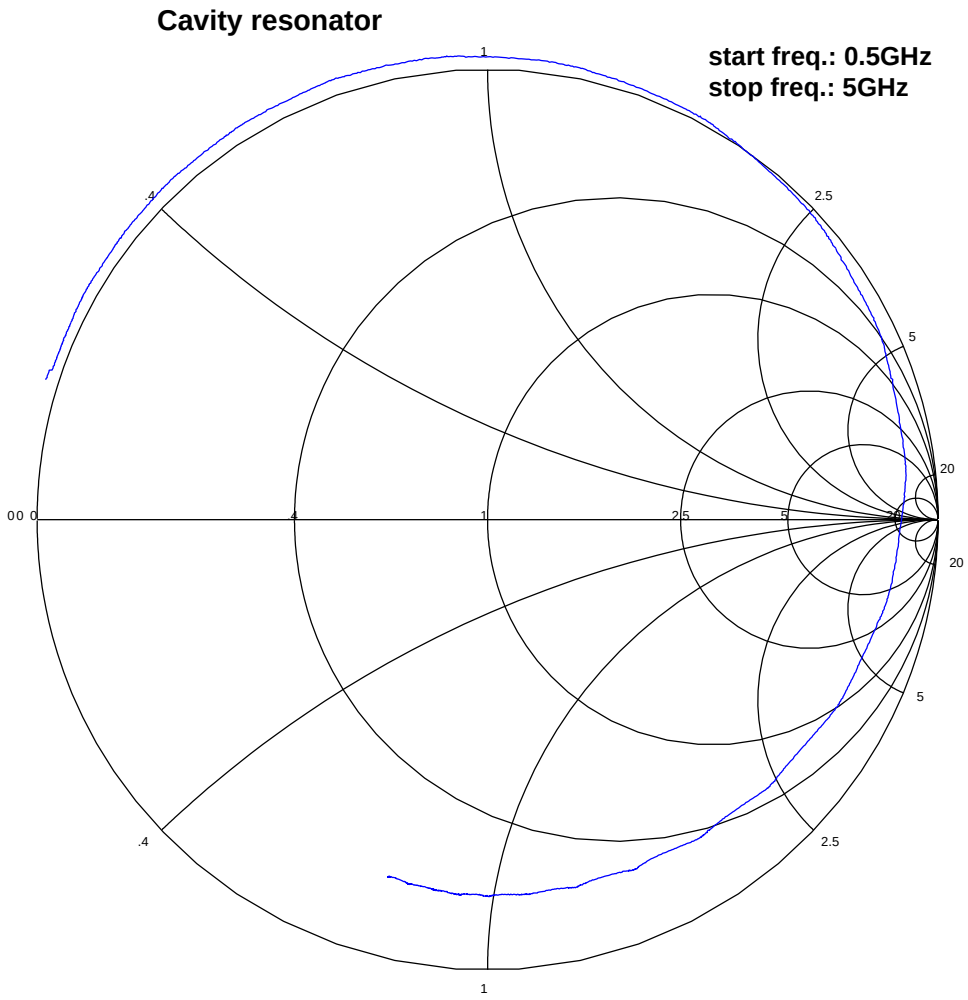


Figure 5.17: Smith chart of the cavity resonator

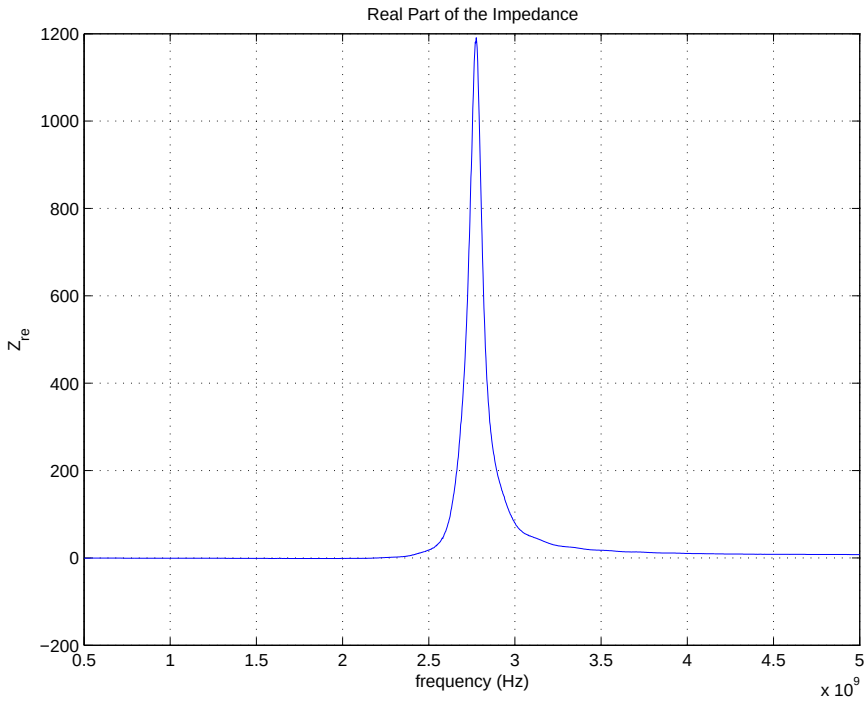


Figure 5.18: Real part of the impedance

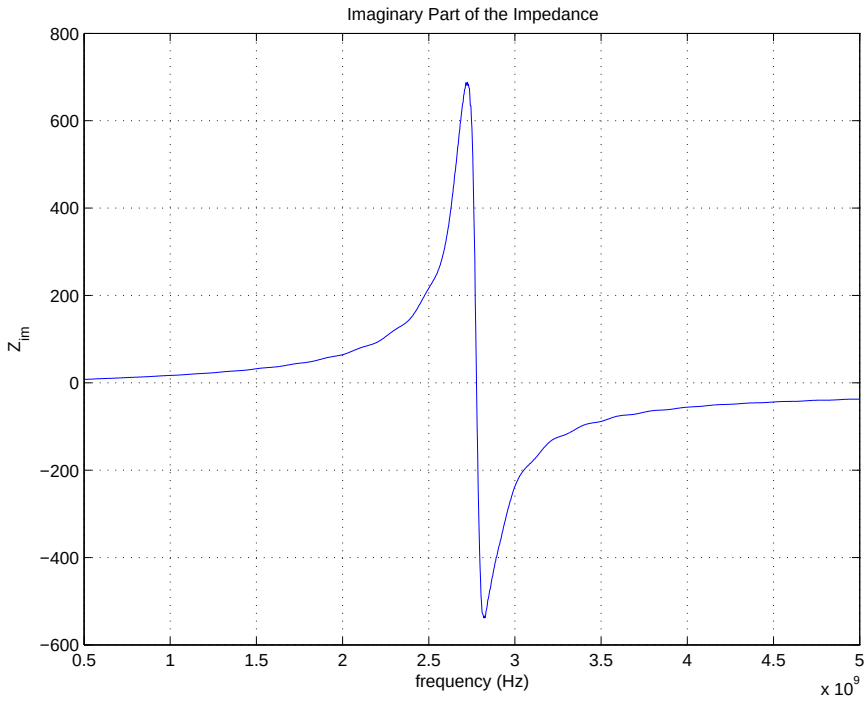


Figure 5.19: Imaginary part of the impedance

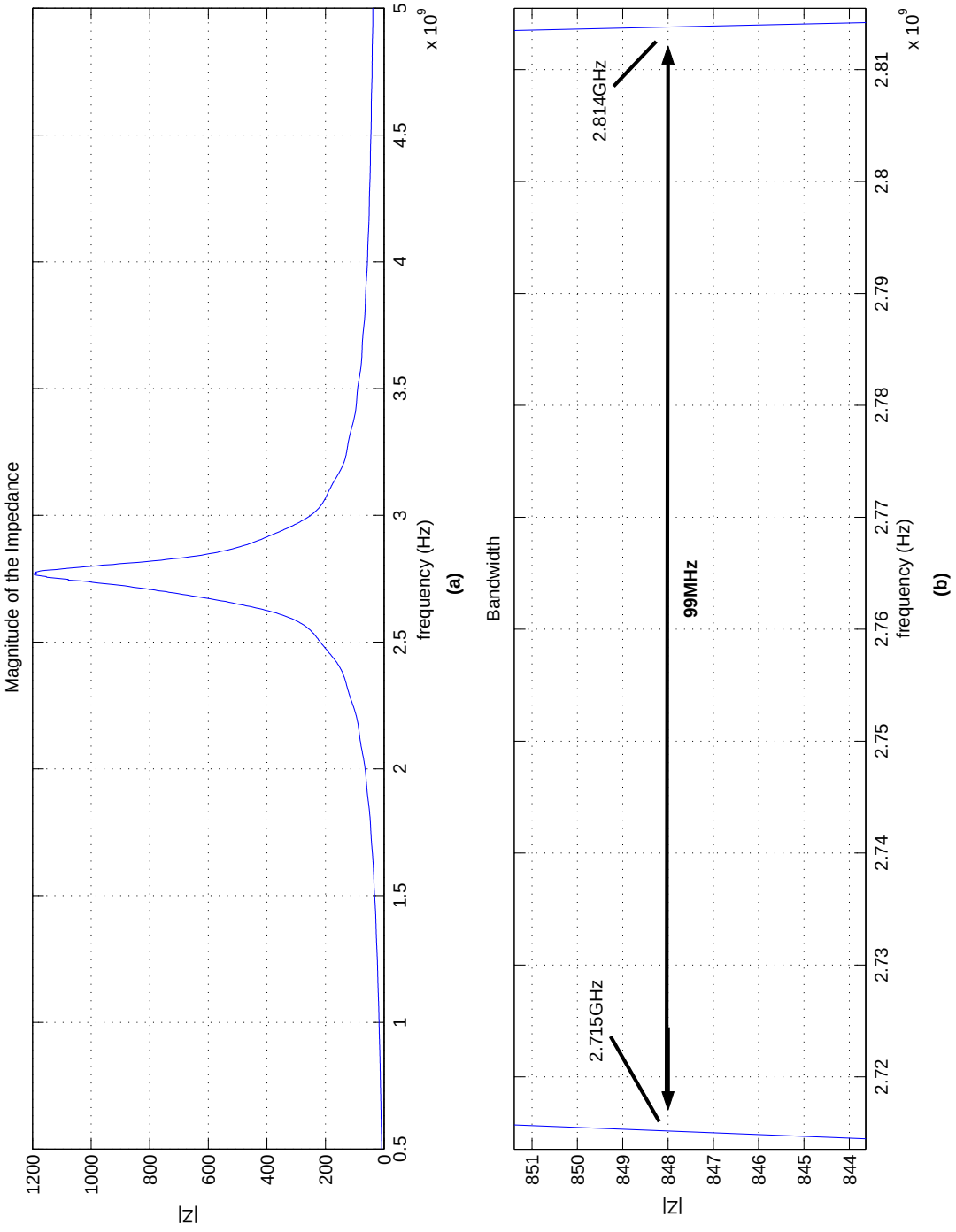


Figure 5.20: (a)Magnitude of the impedance. (b)3dB cut-off frequencies and bandwidth

Chapter 6

CONCLUSIONS and FUTURE WORK

Several conclusions can be drawn from the measurements of the resonator. The primary conclusion is that based on the design and fabrication techniques presented in this thesis, high-Q resonator can be realized at radio-frequencies. The resonance frequency of the fabricated device was measured as 2.78 GHz and the associated Q-factor at the resonance was found as 28. The measurements of the MIM capacitor shows that the loss mechanism inside the capacitor limits the performance of the resonator. The quality factor of the inductor was found much greater than that of the capacitor. So the situation was reversed here. As it is mentioned in the introduction part, at microwave frequencies, capacitors generally exhibit higher quality factor than that of the inductors. Therefore, if the capacior loss is reduced, resonators with higher Q-factors can be realized. The loss due to the parasitic shunt resistance of the dielectric can be reduced by using another dielectric material, which has a lower loss tangent. And the loss due to the series resistance of the electrodes, can be reduced by depositing much thicker metal film. Other practical limitations that have an effect on the quality factor of the resonator, are epoxy bonding of the substrates and bonding

of a round wire. Conductive epoxy, certainly, causes ohmic loss due to the contaminants it contains. Thermocompression bonding can be employed in order to bond two metal coated surfaces to each other. Ribbon wire can be preferred rather than a round wire so that the surface area of the wire is greatly enhanced. If ribbon wire is not available, a larger radius round wire would be convenient to use. Lastly, since the processes are employed on both side of the substrate, double side polished wafers should be used in order to increase the yield to make fabrication easier. The quality factor of the resonator can be greatly enhanced, if these improvements are implemented. Also, note that, the resonance frequency of the device, can be easily adjusted by changing the physical dimensions of the capacitor and inductor during device fabrication. In addition to the MIM capacitor, a varactor can also be fabricated on top of the cavity so that the structure becomes tunable high-Q resonator.

During the fabrication of capacitor, BCB and Si_3N_4 was tested for the dielectric layer. Both materials are low-loss at high frequencies. However, in our measurements, Si_3N_4 exhibited better performance, therefore, it was preferred in the following steps of the fabrication. BCB was not fully examined and capacitor measurements do not imply BCB is a poor dielectric. Here, the main focus is to realize a cavity, not a high-Q MIM capacitor at the top of the substrate.

It is worthwhile to mention here that one of the difficulties that we encountered during the measurements was the calibration of the ports of the network analyzer. The error at the delay calibration reflected to the measurements as a change in the measured inductance value. But, more important than that, the difficulties of measuring a low-loss circuit using a standard network analyzer created a lot of problems. In some measurements, the reflection coefficients from the load was measured as greater than one as shown in figure 5.17. This problem is caused by the imperfect nature of the calibration kit used during calibration of the network analyzer. Obviously, the resonators fabricated had greater reflection

coefficients than the short and open standards of the calibration kit provided at some frequencies. It is difficult to estimate the extent of the uncertainty caused by this problem because we have no idea on the actual reflection coefficients of the calibration kit. But it can be reasonably said that the impedance measurements becomes very much blurred as approaching the unity reflection coefficient circle. Therefore, it seems that different methods should be used for measuring the quality factors of high-Q resonators with Q-factors higher than approximately 20-30 at microwave frequencies.

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